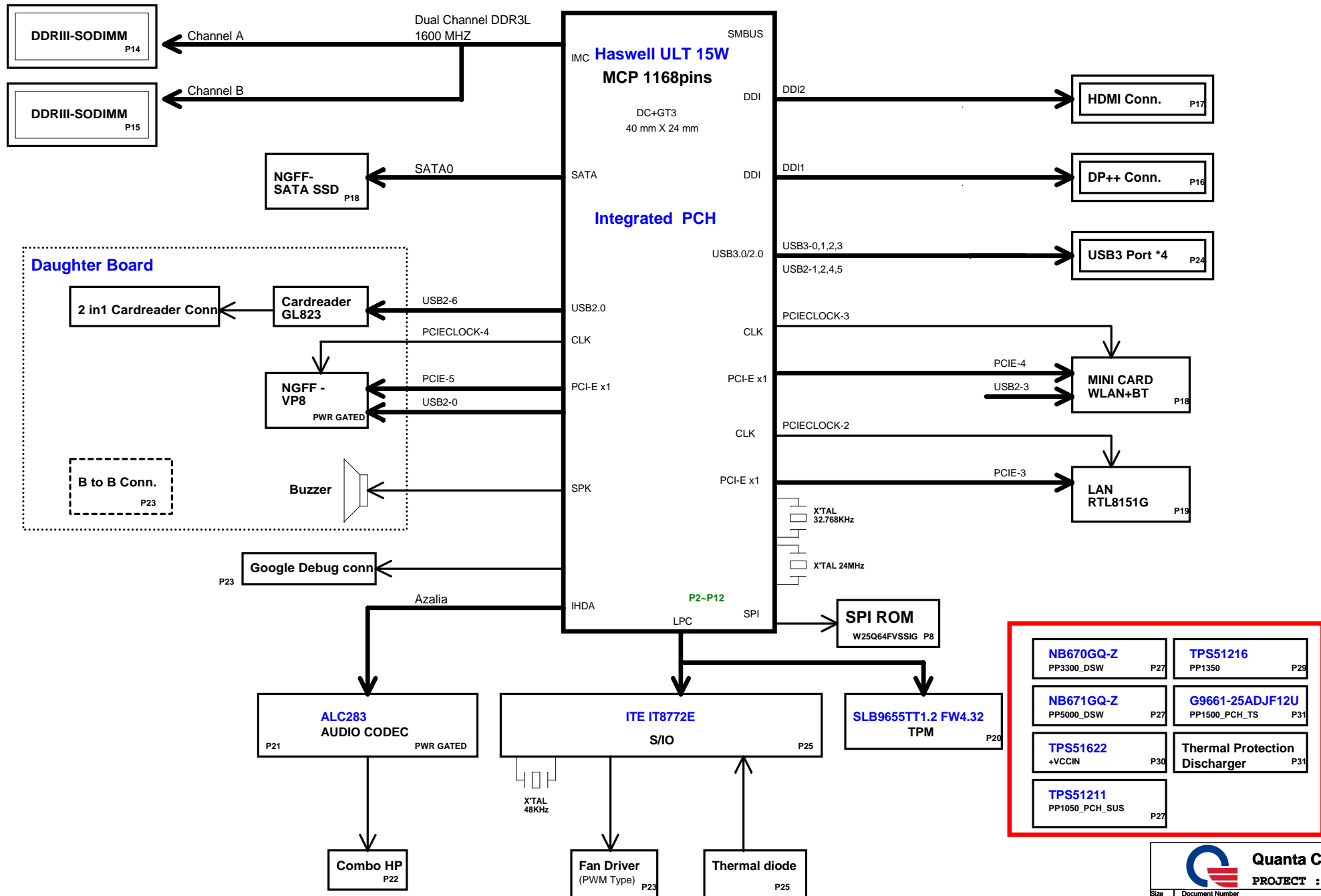
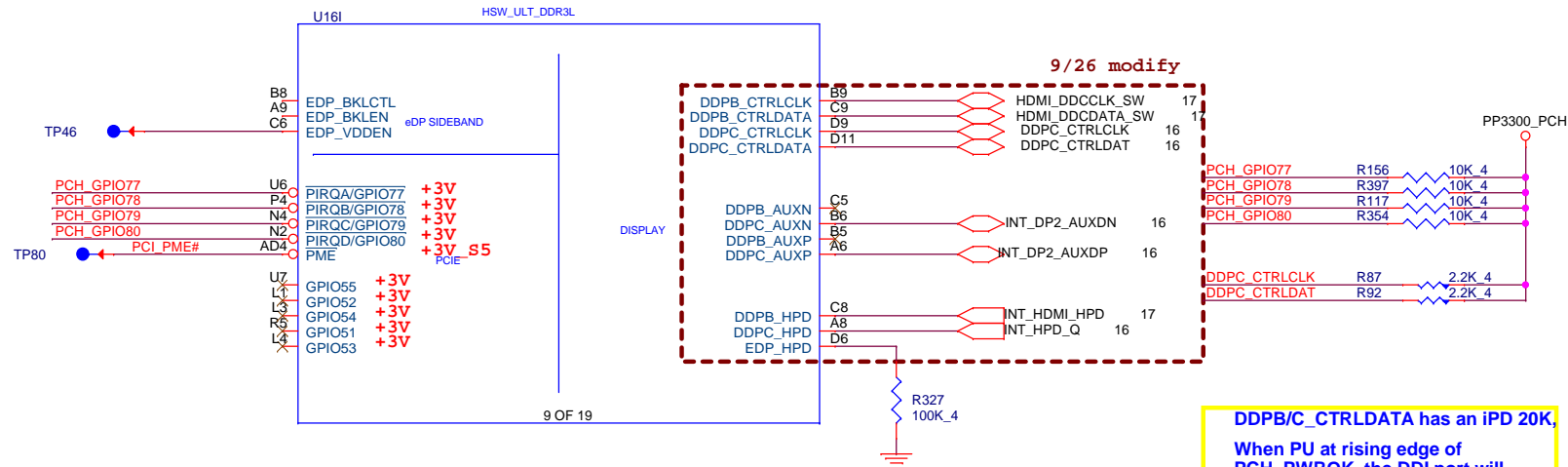
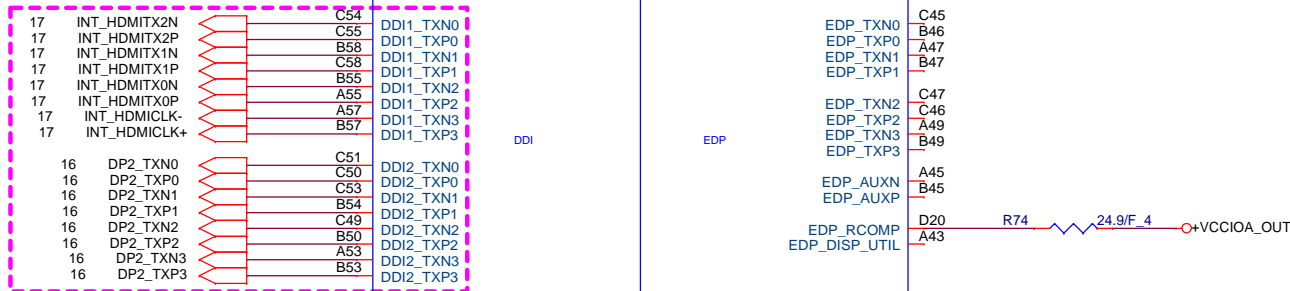


# ZAKO/0W9 SHB ULT SYSTEM BLOCK DIAGRAM



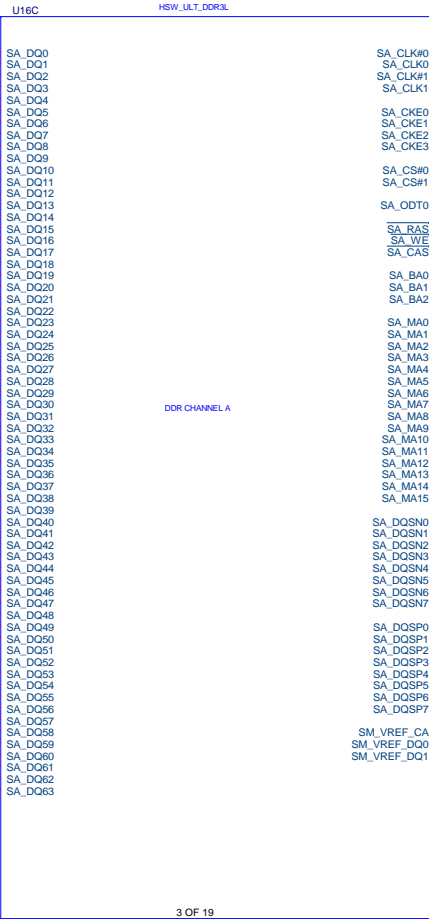
The diagram illustrates the connections for the HSW\_ULI\_TDR3L component. It is divided into two main sections by a vertical line. The left section, labeled 'U16A' at the top, contains a dashed pink box listing the following components: DDI1\_TXN0, DDI1\_TXP0, DDI1\_TXN1, DDI1\_TXP1, DDI1\_TXN2, DDI1\_TXP2, DDI1\_TXN3, DDI1\_TXP3, DDI2\_TXN0, DDI2\_TXP0, DDI2\_TXN1, DDI2\_TXP1, DDI2\_TXN2, DDI2\_TXP2, DDI2\_TXN3, and DDI2\_TXP3. The right section, labeled 'HSW\_ULI\_TDR3L' at the top, lists the following components: EDP\_TXN0, EDP\_TXP0, EDP\_TXN1, EDP\_TXP1, EDP\_TXN2, EDP\_TXP2, EDP\_TXN3, EDP\_TXP3, EDP\_AUXN, EDP\_AUXP, EDP\_RCOMP, and EDP\_DISP\_UTIL. A vertical line separates the two sections. A horizontal line connects the dashed pink box to the 'DDI' label. Another horizontal line connects the right section to the 'EDP' label. A vertical line connects the 'DDI' label to the 'EDP' label.

9/23 modify



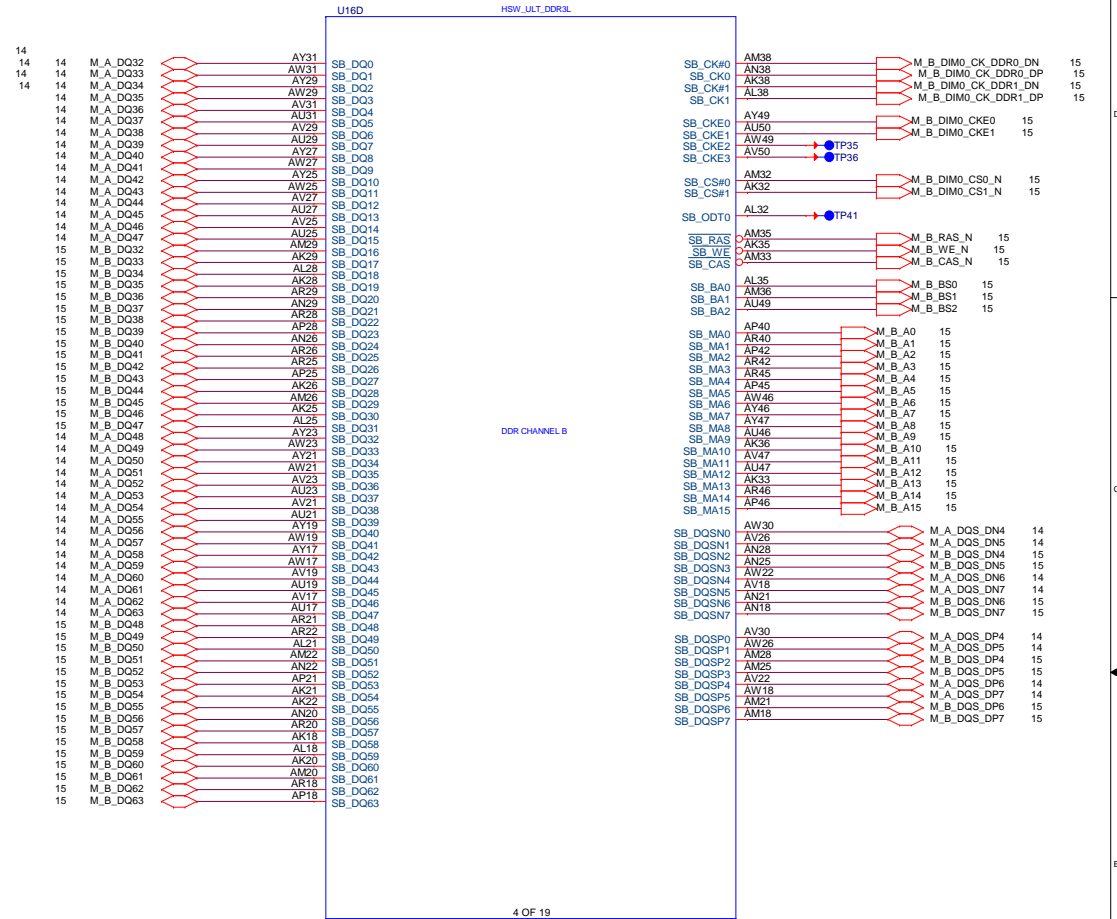
DDPB/C\_CTRLDATA has an iPD 20K,  
When PU at rising edge of  
PCH\_PWROK, the DDI port will  
be detected

# Haswell ULT (DDR3L)



3 OF 19

# Haswell Processor (DDR3L)

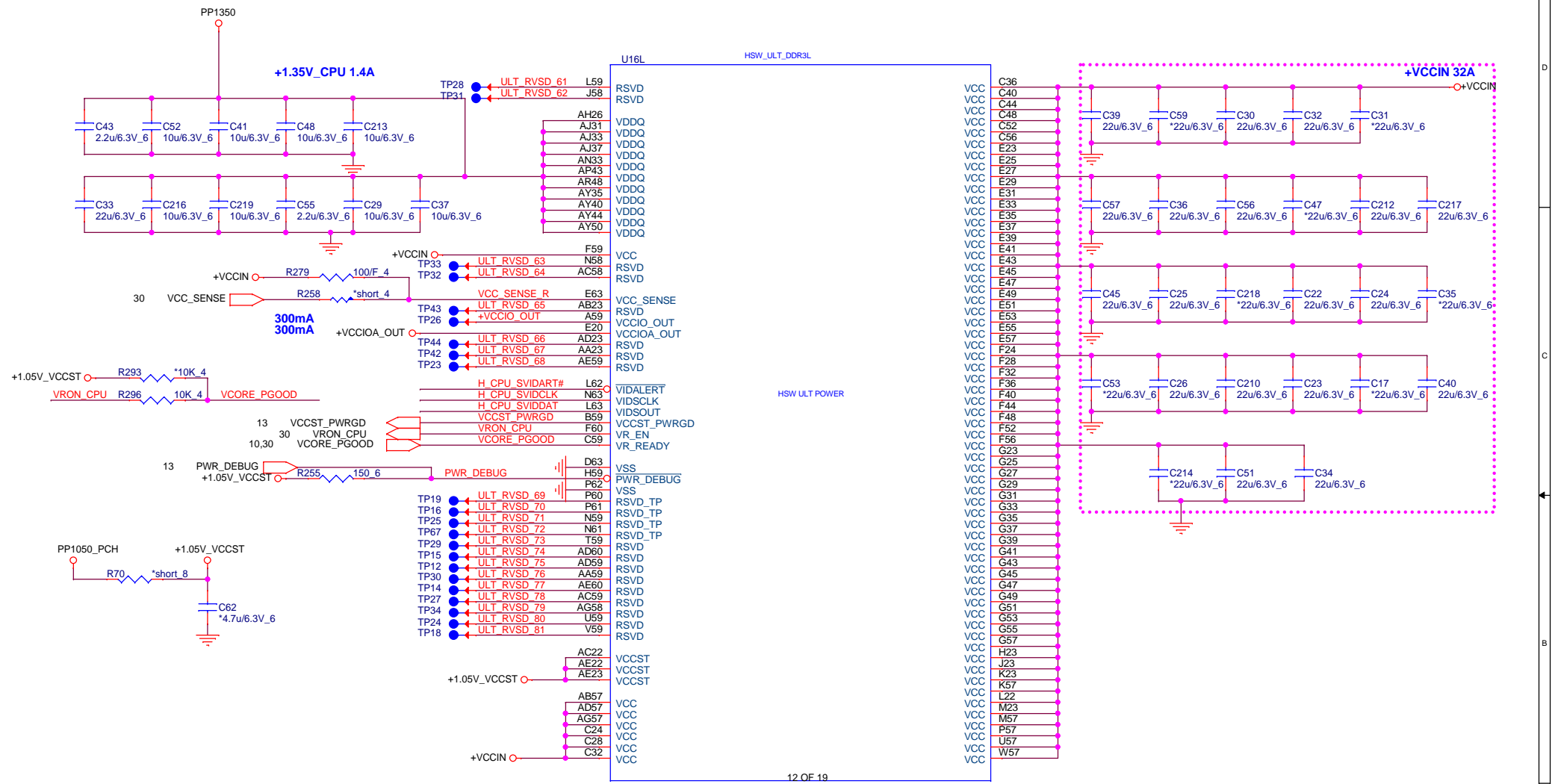


4 OF 19

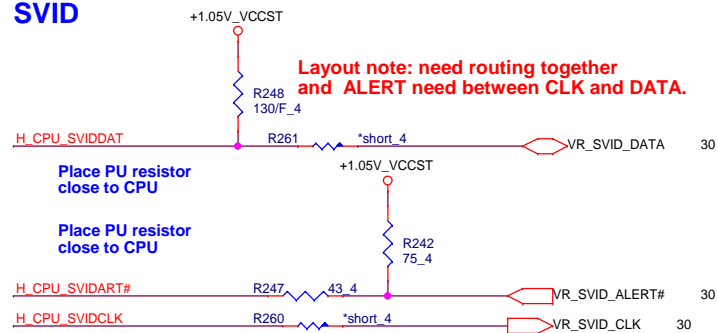
**BPM#[0:7]**  
Trace Length 1~6 inches  
Length match < 300 mils

Size	Document Number <b>Haswell 3/5 (SideBand)</b>	Rev 3A
Date:	Monday, March 31, 2014	Sheet 4 of 33

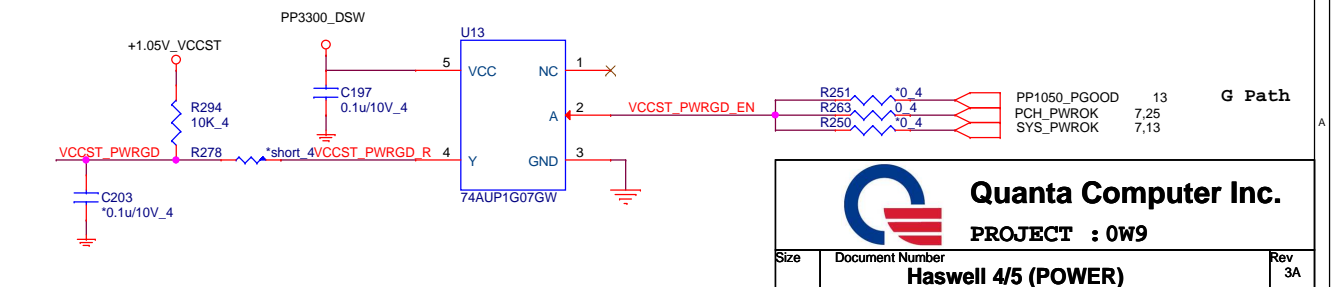
## Haswell ULT (POWER)



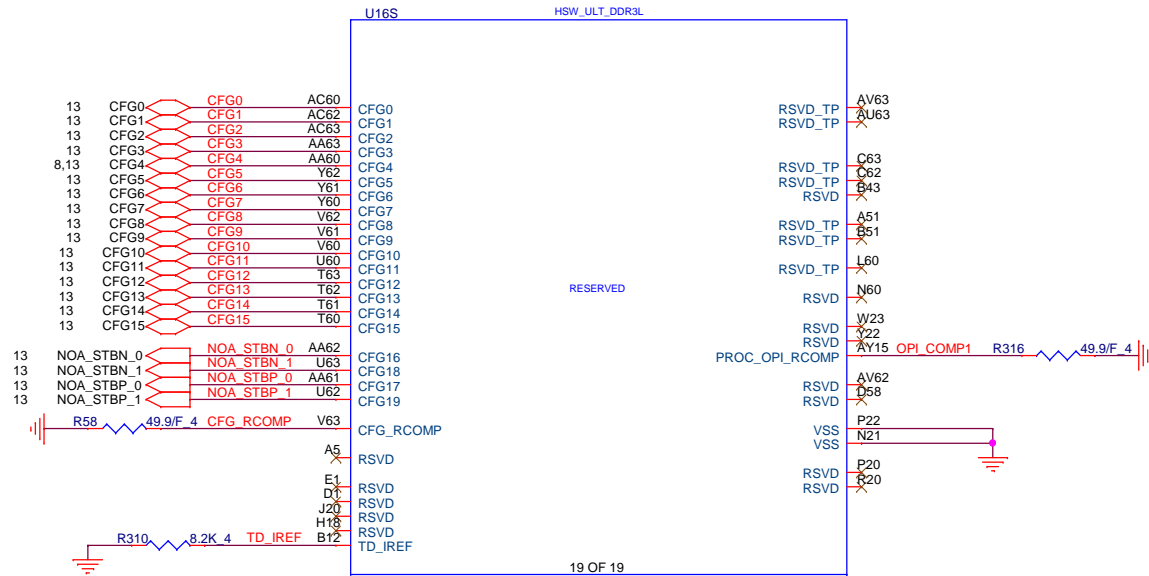
## SVID



## VCCST PWRGD



# Haswell ULT (CFG,RSVD)



## Processor Strapping

	1	0	
CFG0 EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKED	(DEFAULT) NORMAL OPERATION; NO STALL	STALL	CFG0 R268 *1K 4
CFG1 PCH/ PCH LESS MODE SELECTION	(DEFAULT) NORMAL OPERATION	PCH-LESS MODE	CFG1 R264 *1K 4
CFG3 PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT	ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT	CFG3 R265 *1K 4
CFG 8 ALLOW THE USE OF NOA ON LOCKED UNITS	DISABLED(DEFAULT); IN THIS CASE, NOA WILL BE DISABLED IN LOCKED UNITS AND ENABLED IN UN-LOCKED UNITS	ENABLED; NOA WILL BE AVAILABLE REGARDLESS OF THE LOCKING OF THE UNIT	CFG8 R53 *1K 4
CFG9 NO SVID PROTOCOL CAPABLE VR CONNECTED	VRS SUPPORTING SVID PROTOCOL ARE PRESENT	NO VR SUPPORTING SVID IS PRESENT. THE CHIP WILL NOT GENERATE (OR RESPOND TO) SVID ACTIVITY	CFG9 R54 *1K 4
CFG10 SAFE MODE BOOT	POWER FEATURES ACTIVATED DURING RESET	POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED	CFG10 R50 *1K 4

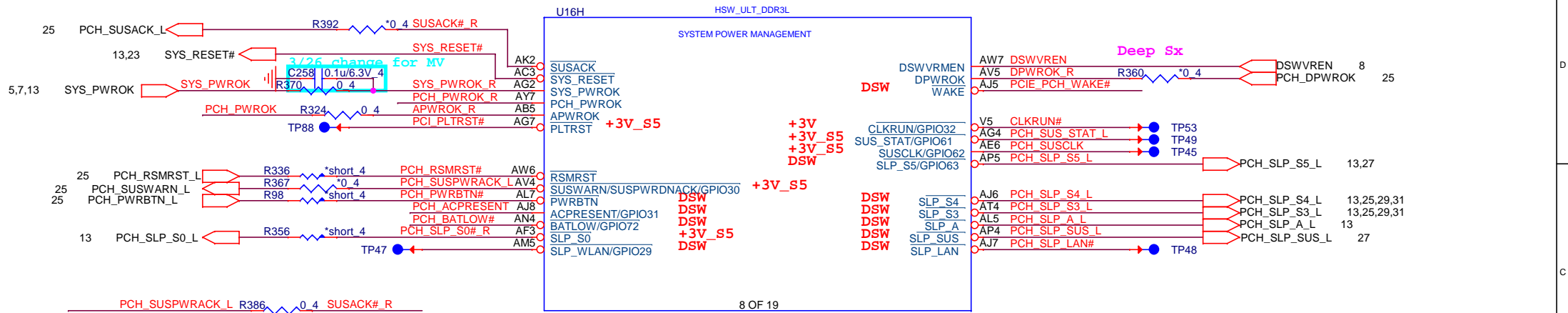


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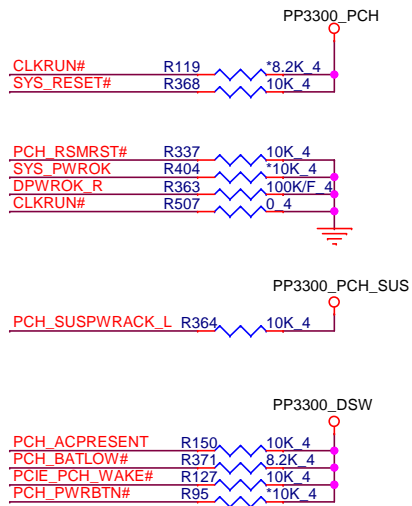
PROJECT : 0W9

Size	Document Number	Rev
	Haswell 5/5 (CFG/GND)	3A
Date:	Monday, March 31, 2014	Sheet 6 of 33

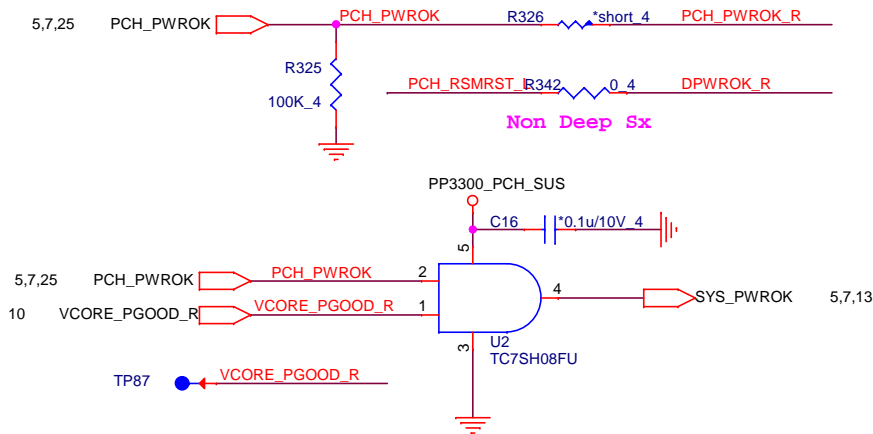
# Haswell ULT PCH (PM)



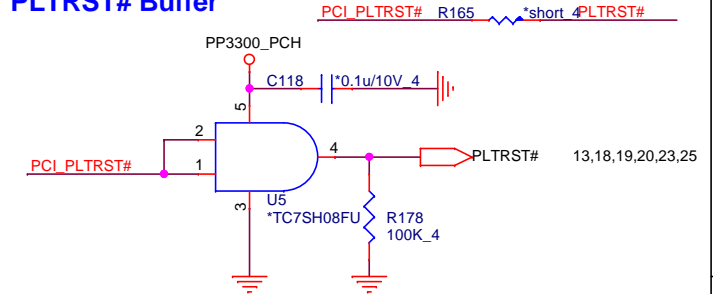
## PCH PM PU/PD



## PCH PWROK



## PLTRST# Buffer

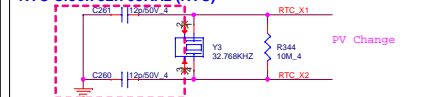


**Quanta Computer Inc.**

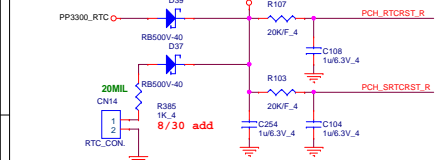
**PROJECT : 0W9**

Size	Document Number	Rev
	<b>PCH 1/6 (PM)</b>	3A
Date:	Monday, March 31, 2014	Sheet 7 of 33

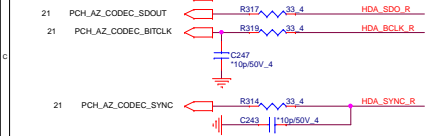
# RTC Clock 32.768KHz (RTC)



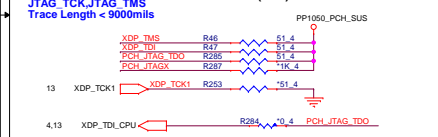
# RTC Circuitry (RTC)



# HDA



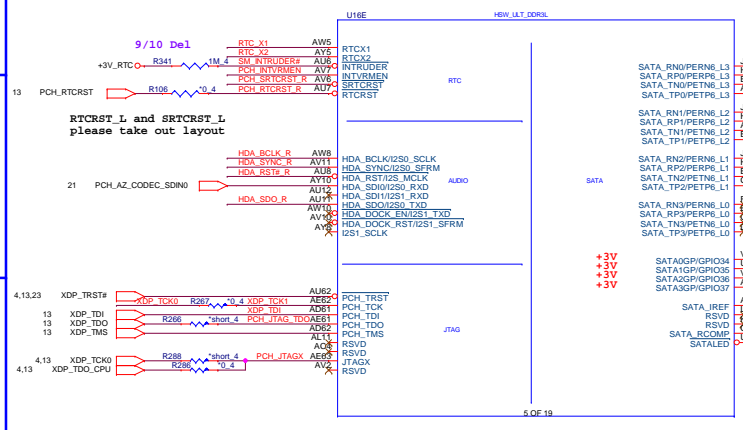
# PCH JTAG



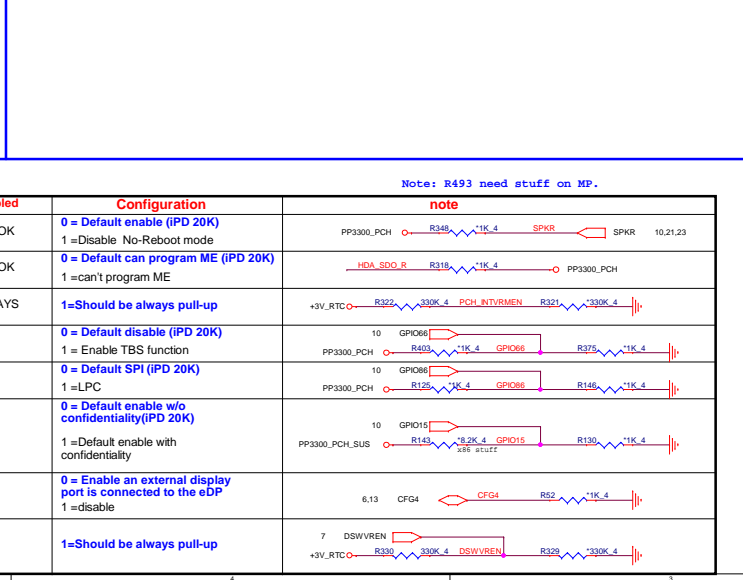
# ULT Strapping Table

Pin Name	Strap description	Sampled	Configuration
GPIO81(SPKR)	No reboot on TCO Timer expiration	PWROK	0 = Default enable (IPD 20K) 1 = Disable No-Reboot mode
HDA_SDO	Flash Descriptor Security Override / Intel ME Debug Mode	PWROK	0 = Default can program ME (IPD 20K) 1 = can't program ME
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	1=Should be always pull-up
GPIO66	Top-Block Swap override		0 = Default disable (IPD 20K) 1 = Enable TBS function
GPIO86	Boot BIOS Strap Bit		0 = Default SPI (IPD 20K) 1 = LPC
GPIO15	TLS(Transport layer security)		0 = Default enable w/o confidentiality(IPD 20K) 1 = Default enable with confidentiality
CFG4	DP presence strap		0 = Enable an external display port is connected to the eDP 1 = disable
DSWVREN	Deep Sx well on the VR enable		1=Should be always pull-up

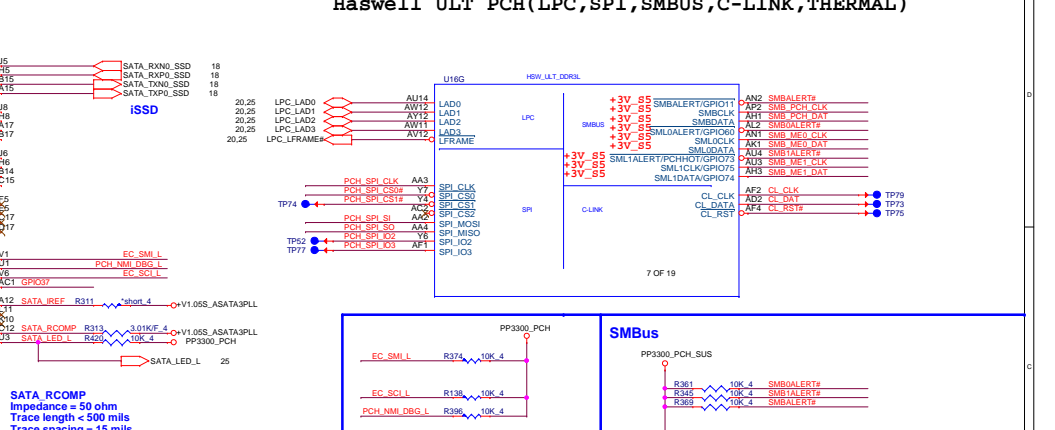
# Haswell ULT PCH (RTC/HDA/SATA/SPI)



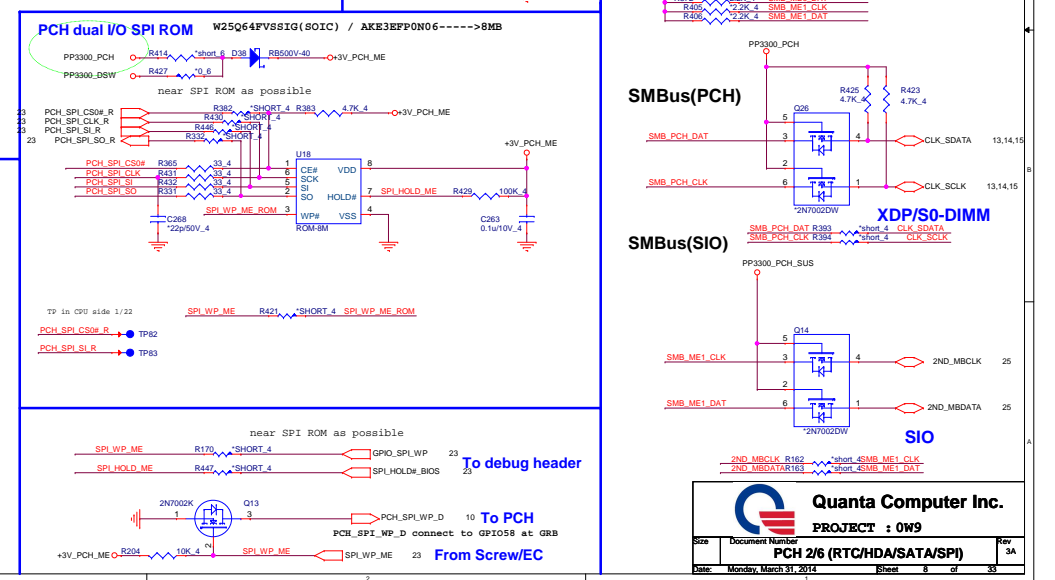
# Haswell ULT PCH(LPC, SPI, SMBUS, C-LINK, THERMAL)



# Haswell ULT PCH (RTC/HDA/SATA/SPI)



# Haswell ULT PCH(LPC, SPI, SMBUS, C-LINK, THERMAL)





[illegible]

Haswell ULT PCH (GPIO,CPU/MISC,NCTF)

U16J HSW\_ULT\_DDR3L

10 OF 19

3/26 change for MV

PP3300\_PCH\_SUS

PP3300\_PCH PP3300\_PCH\_SUS

G Path I Path

R152 \*0.4 R139 0.4

R141 10K 4 PCH\_SPI\_WP\_D R126 10K 4 GPIO14

PP3300\_DSW PP3300\_PCH\_SUS

I Path G Path

R391 0.4 R390 \*0.4

R384 10K 4 RECOVERY\_L

10,18,31 PP3300\_WLAN\_EN 5

WLAN\_WAKE\_L\_Q 3

WLAN\_WAKE\_L 4

10,31 PP3300\_LAN\_EN 2

LAN\_WAKE\_L\_Q 6

LAN\_WAKE\_L 1

2N7002DW

CPU thermal trip

U24 74AUP1G07GW

1 NC VCC 5

2 A 7

3 GND 4

Y

+1.05V\_VCCST

C330 0.1u/10V\_4

R493 10K\_4

PP3300\_PCH

VCORE\_PG00D

VCORE\_PG00D\_R

THRMTRIP#

Q9 FDV301N

Q11 MMBT3904-7-F

SYS\_SHDN# 23,27

PP3300\_PCH

PP3300\_PCH\_SUS

PP3300\_DSW

GPIO27 : If not used then use 8.2-kΩ to 10-kΩ pull-down to GND.

USB\_ILIM\_SEL R128 \*10K 4

PP3300\_SSD\_EN R120 \*10K 4

PP3300\_SSD\_EN R142 100K 4

WLAN\_WAKE\_L\_Q R440 \*short 4

LAN\_WAKE\_L\_Q R175 \*short 4

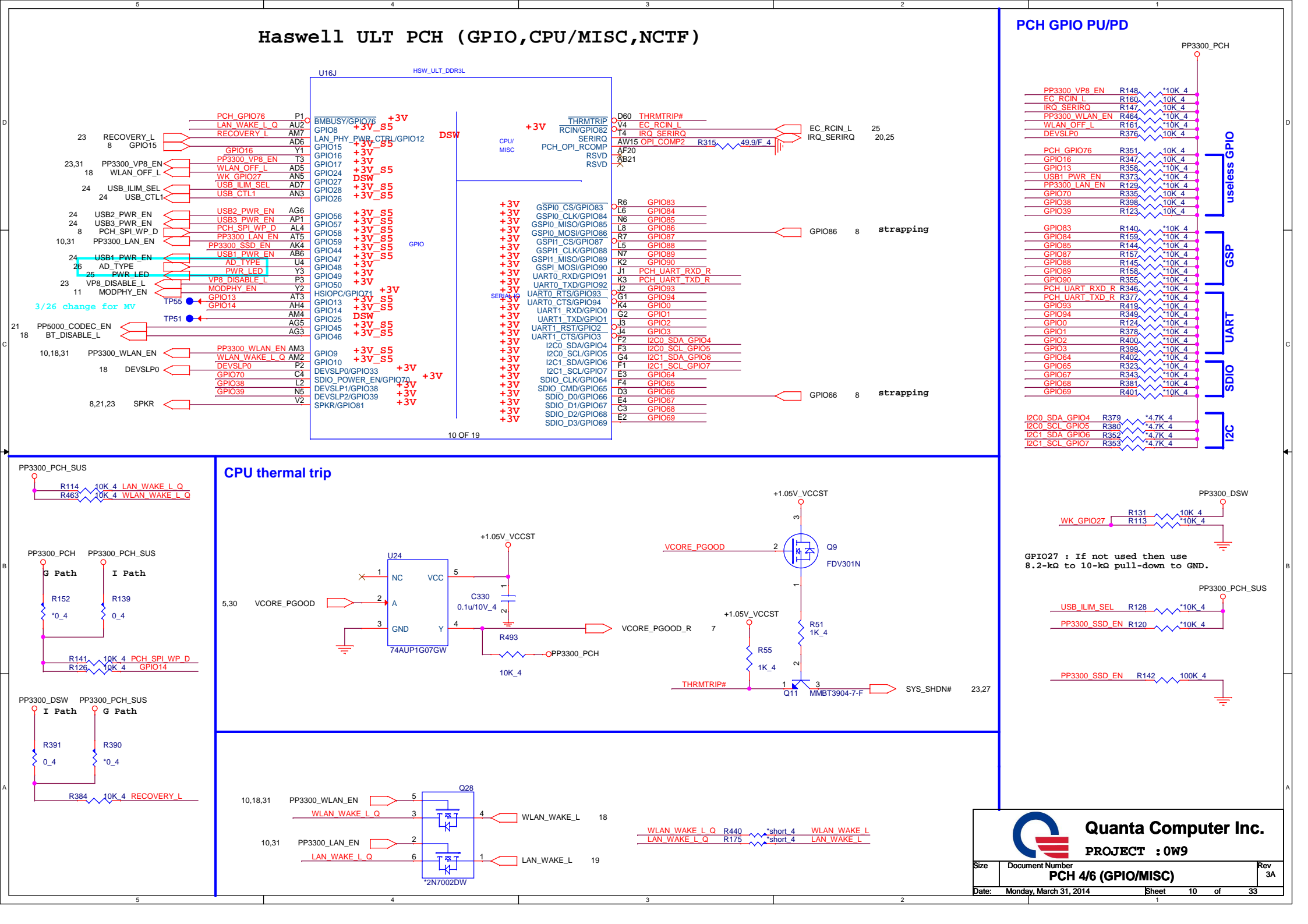
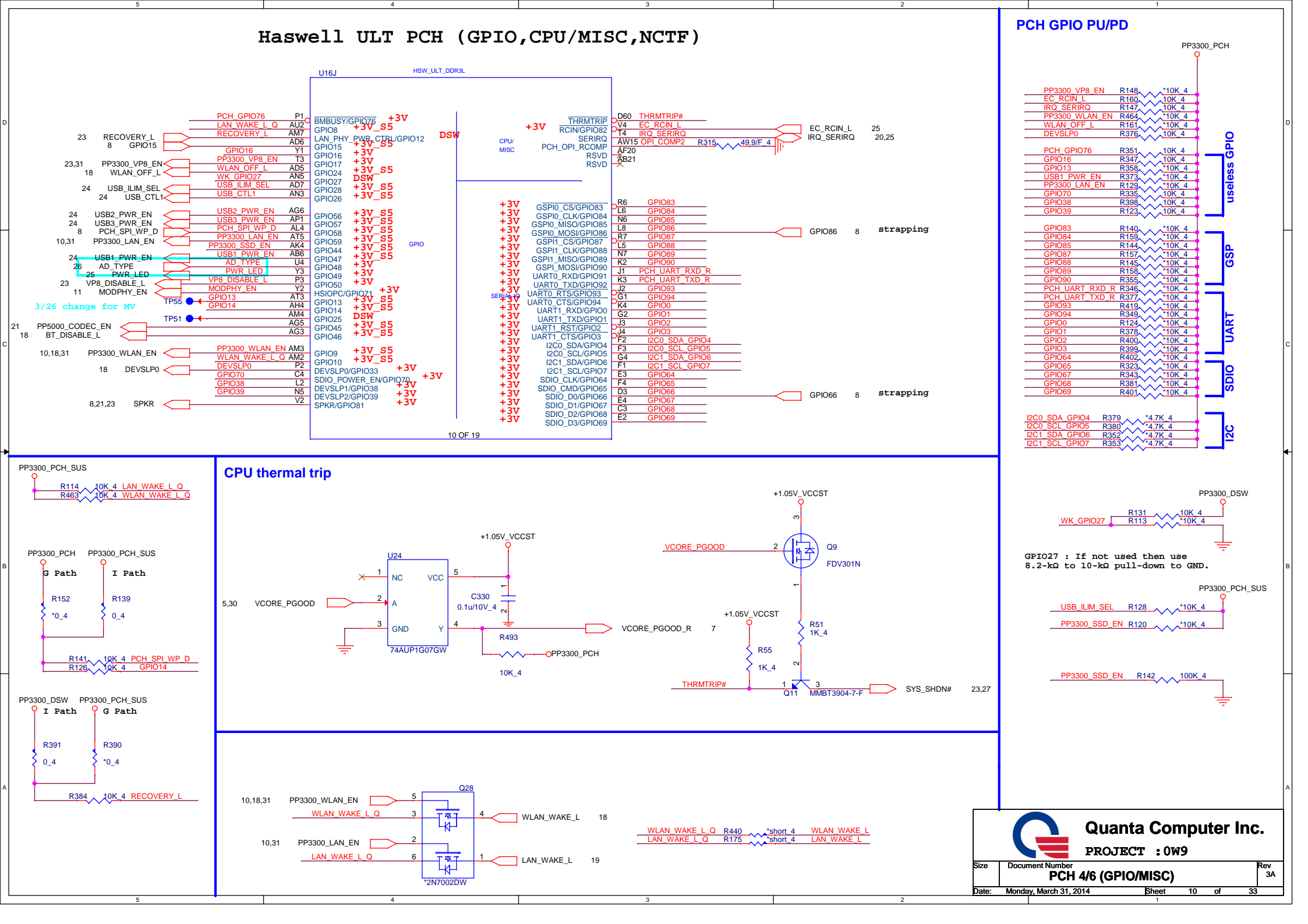
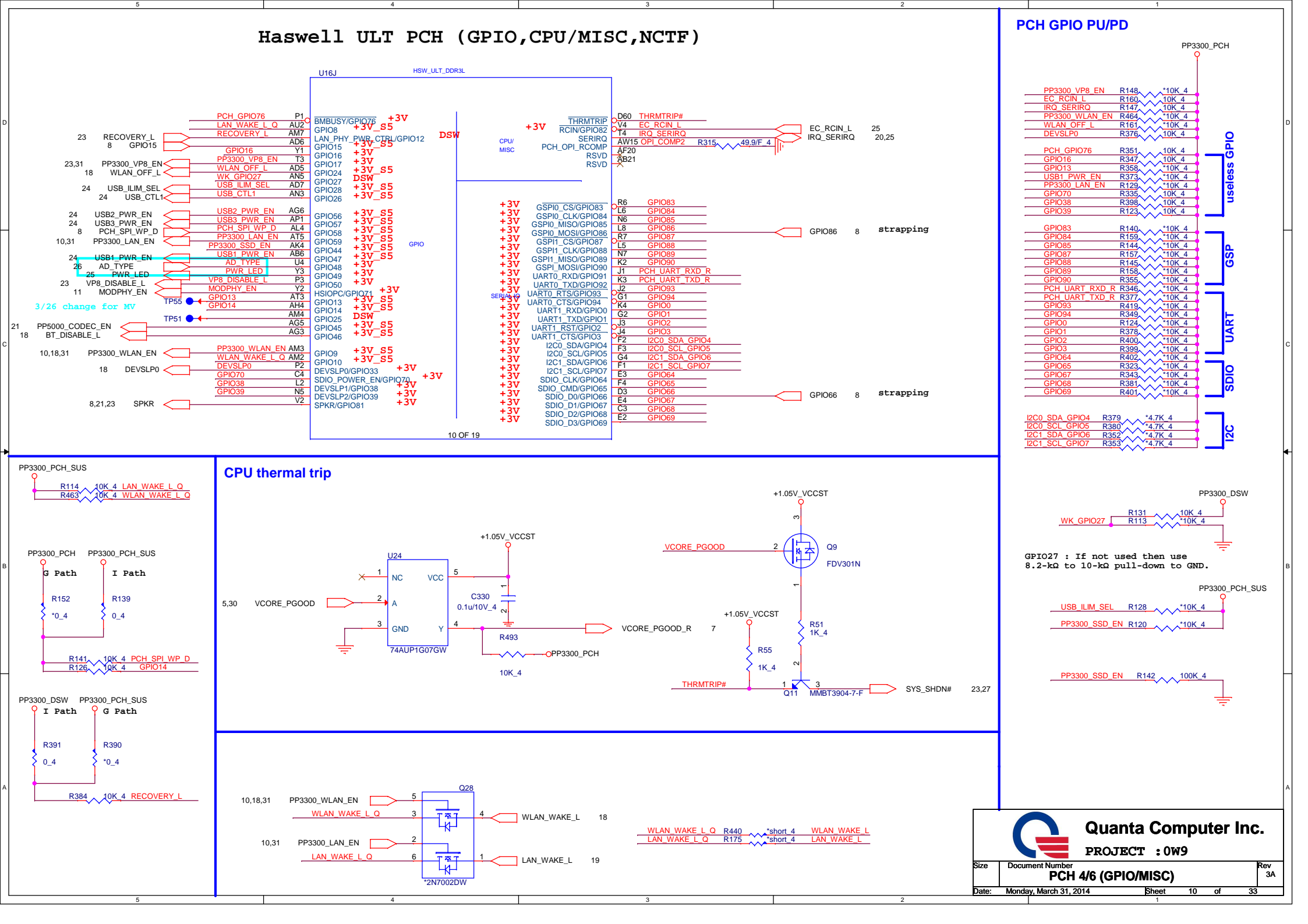
WLAN\_WAKE\_L LAN\_WAKE\_L

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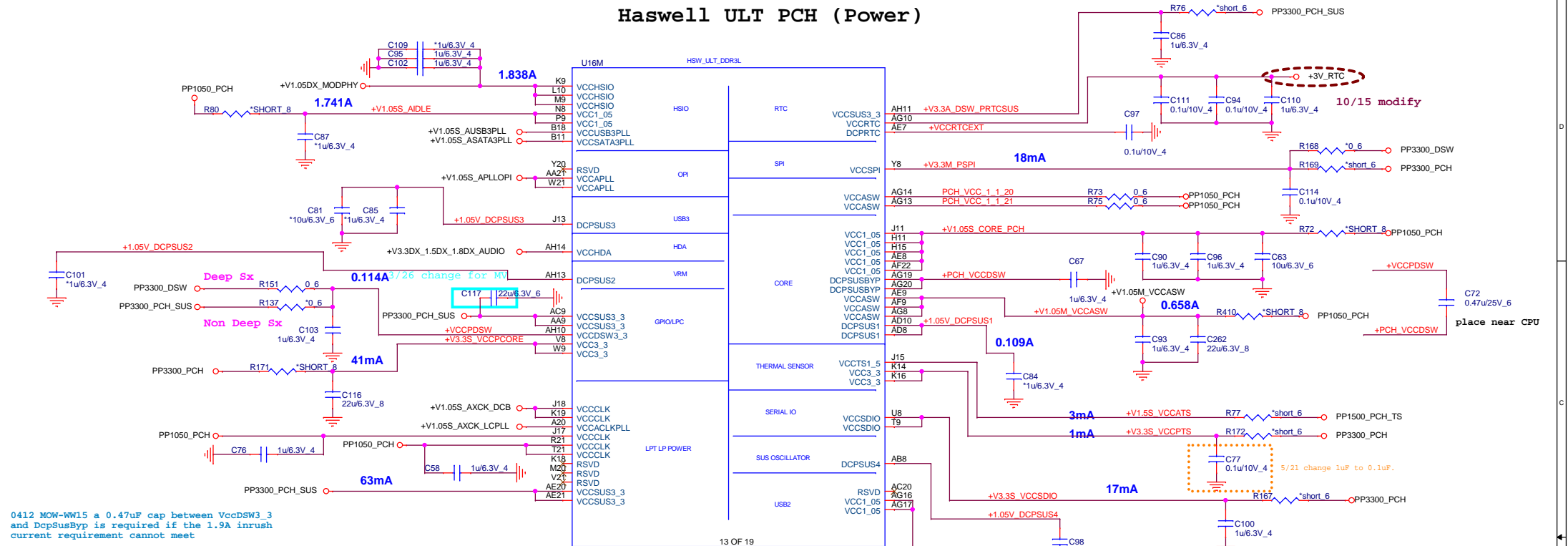
PROJECT : 0W9

Size Document Number PCH 4/6 (GPIO/MISC) Rev 3A

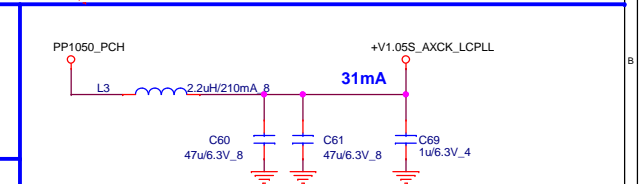
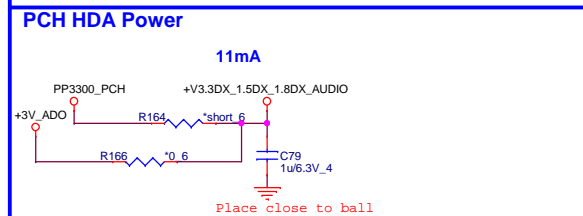
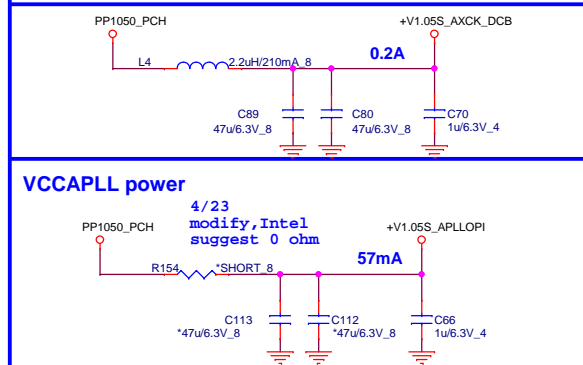
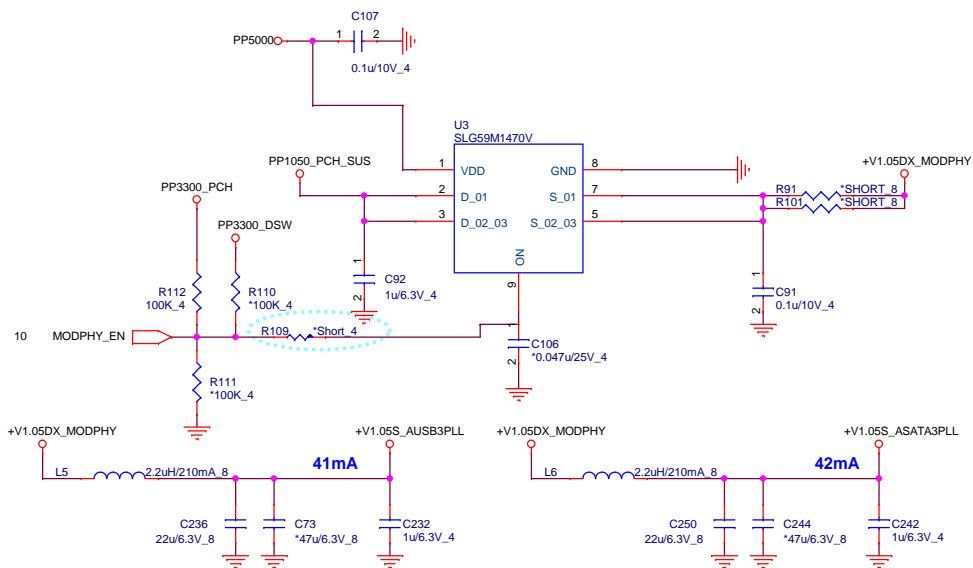
Date: Monday, March 31, 2014 Sheet 10 of 33

[illegible][illegible]

## Haswell ULT PCH (Power)



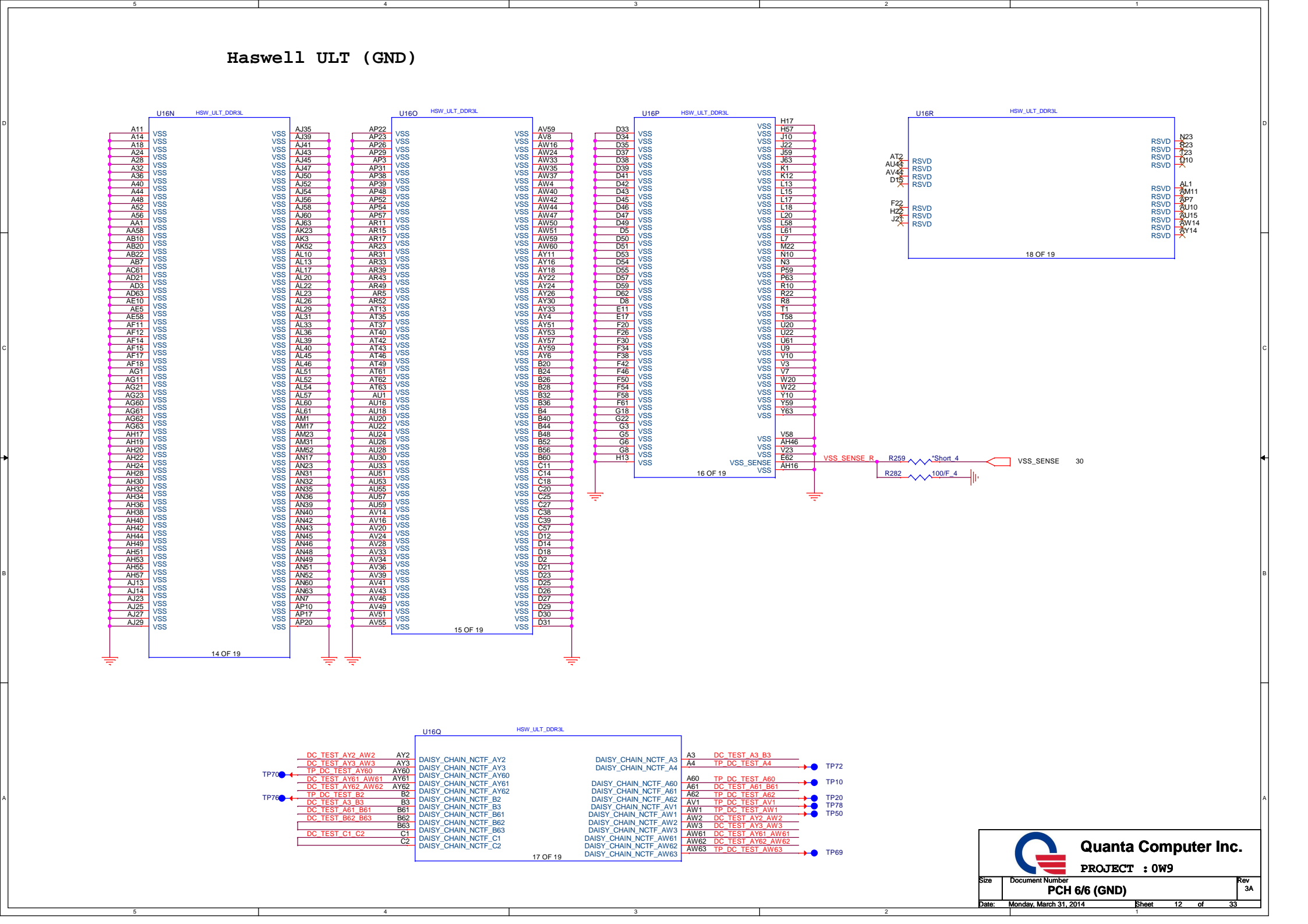
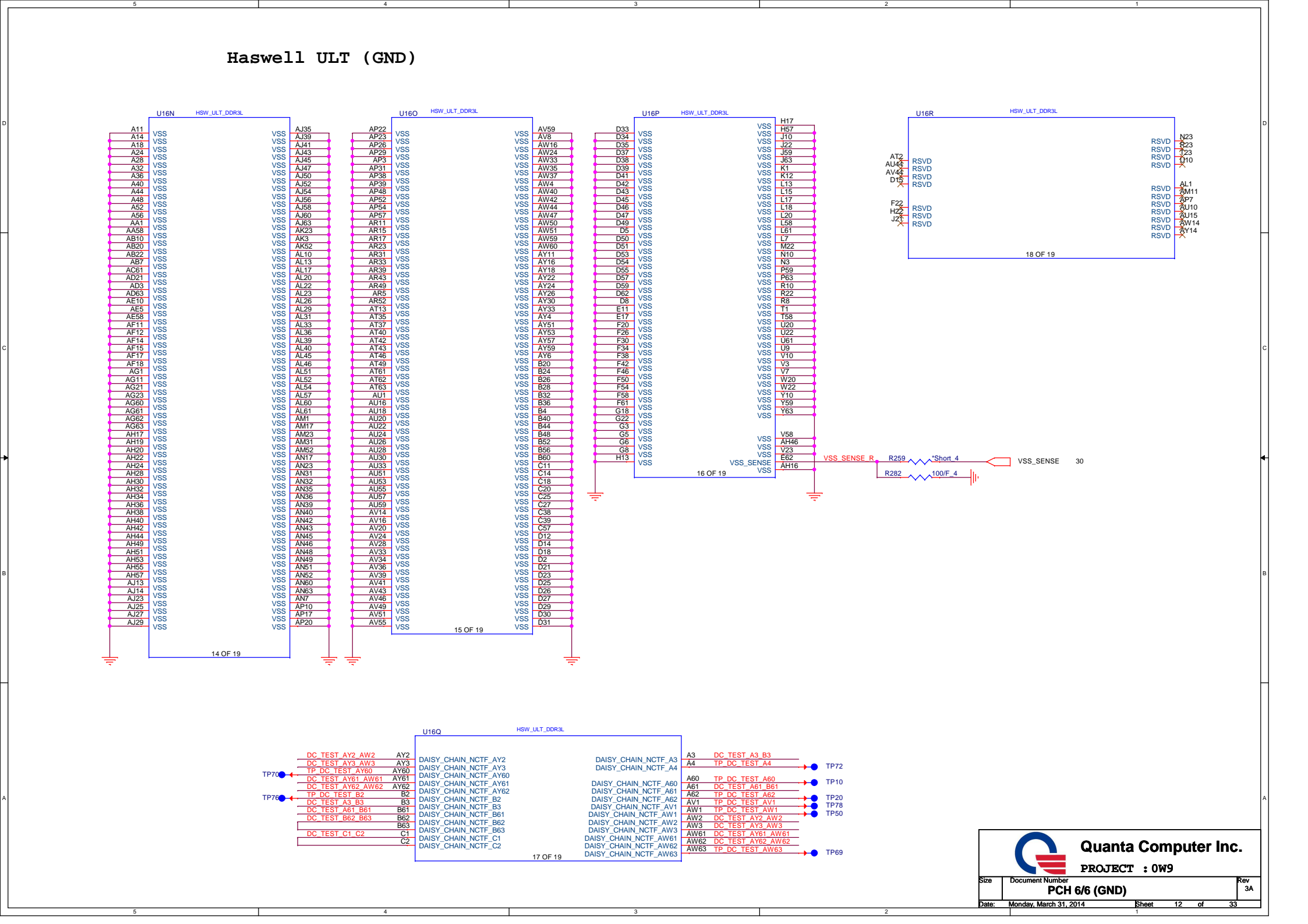
## PCH VCCHSIO Power

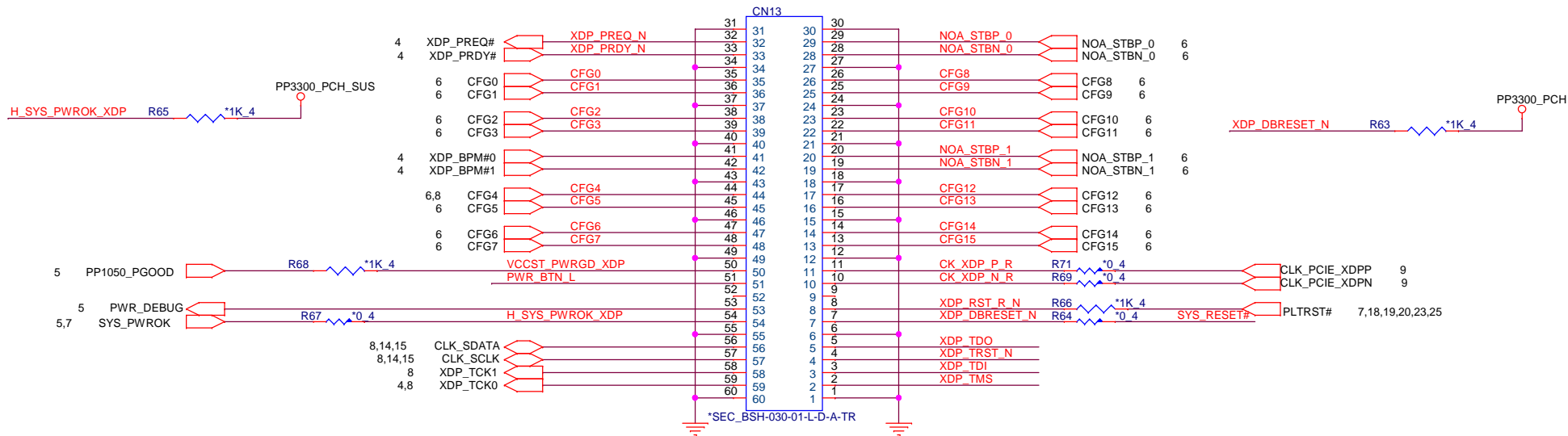
**Quanta Computer Inc.**

PROJECT : 0W9

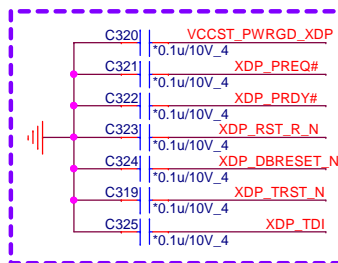
## PCH 5/6 (POWER)

Size	Document Number <b>PCH 5/6 (POWER)</b>	Rev 3A
Date:	Monday, March 31, 2014	Sheet 11 of 33

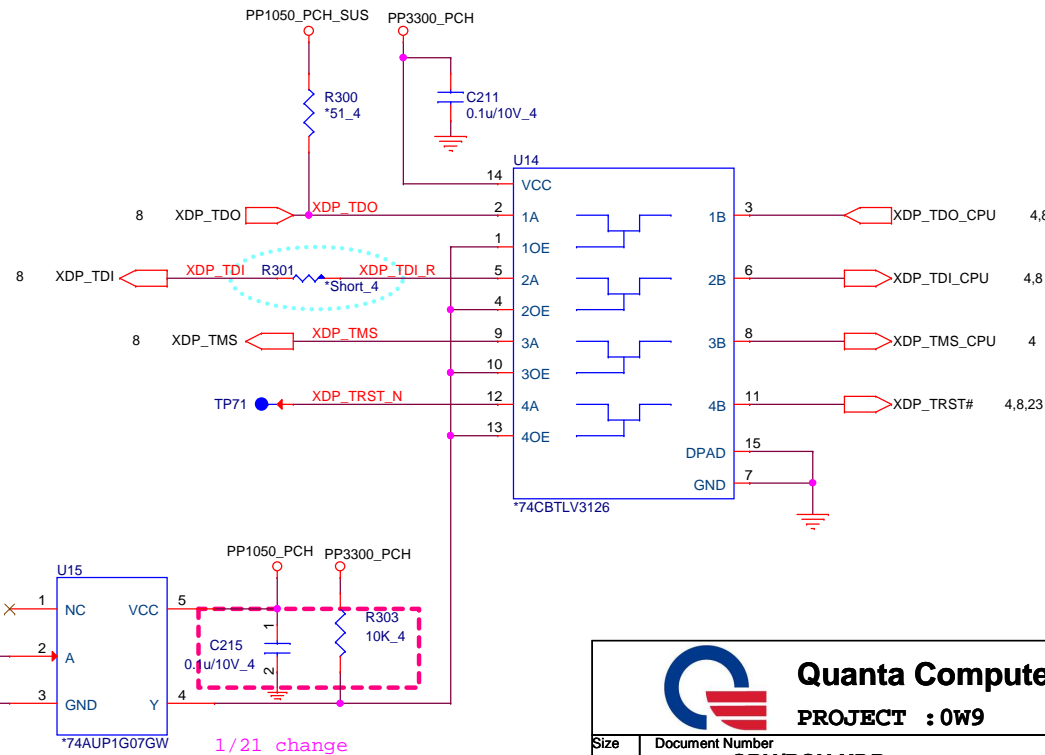
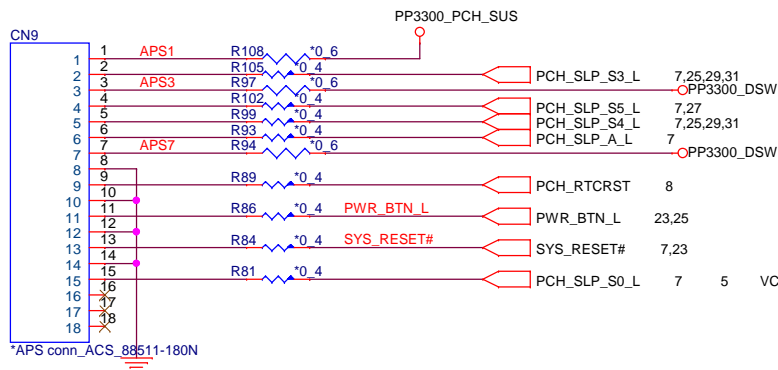
[illegible]



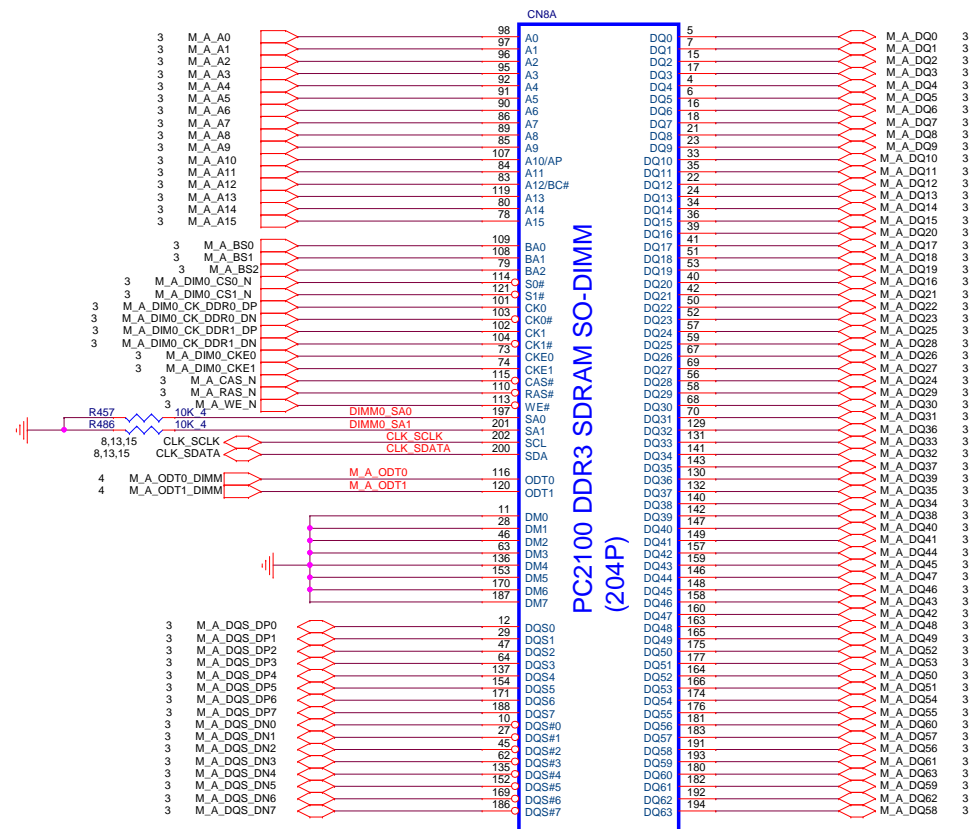
9/30 add for EMI



APS

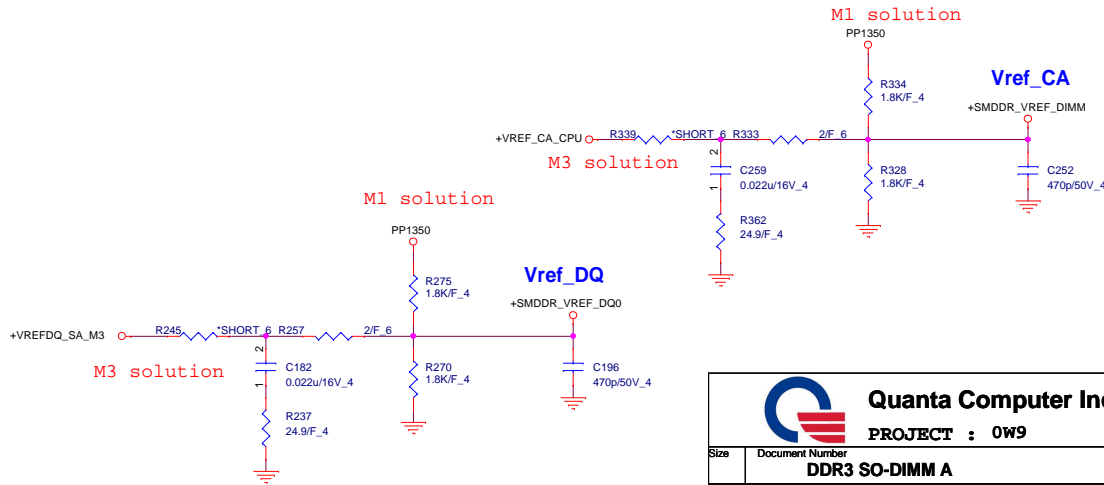
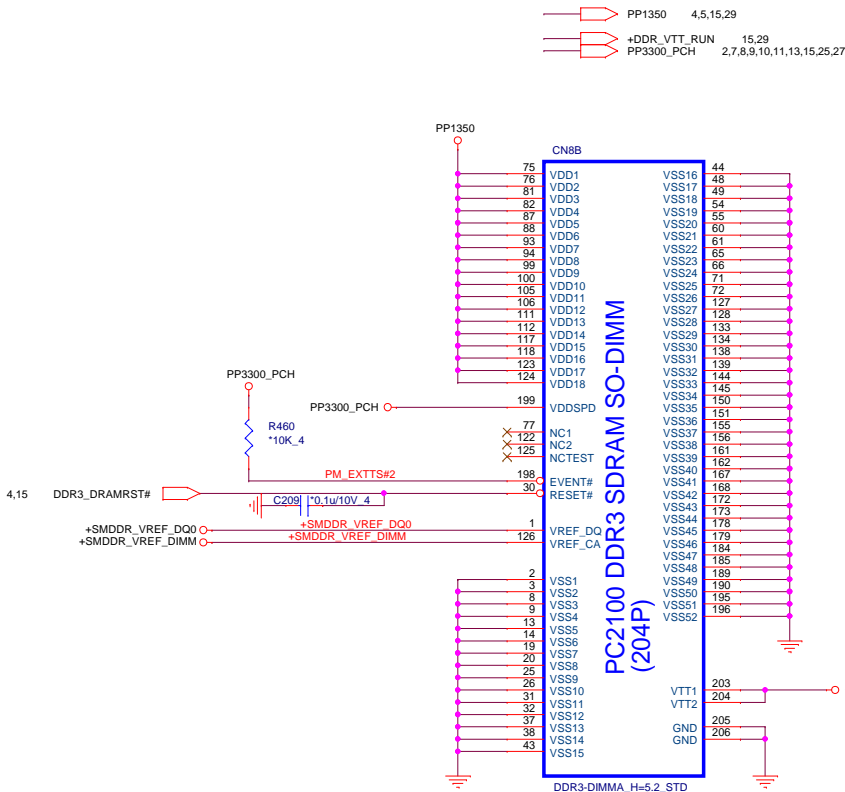
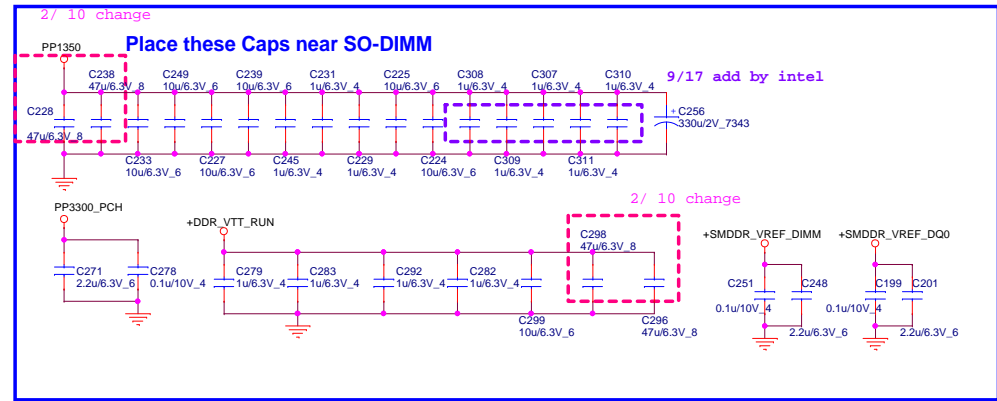


## DDR3 DIMM-A



SM_MEM BUS ADDRESS	
SO-DIMM0	1010 000
SO-DIMM1	1010 001

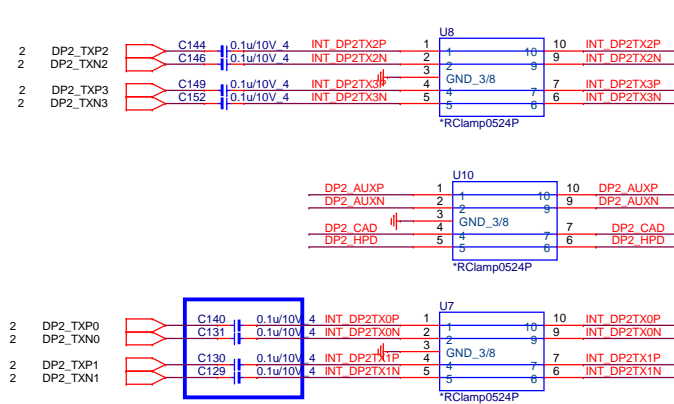
**Place these Caps near So-Dimm A**



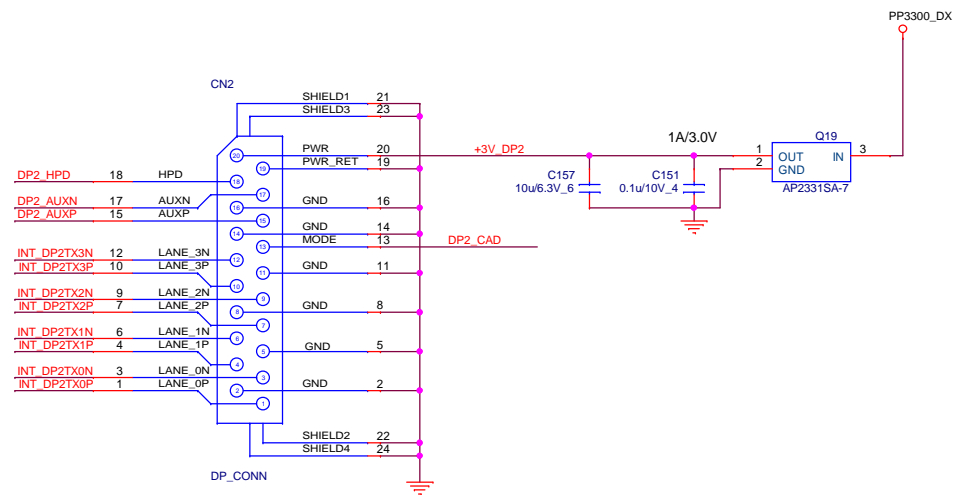




## DisplayPort (DPP)

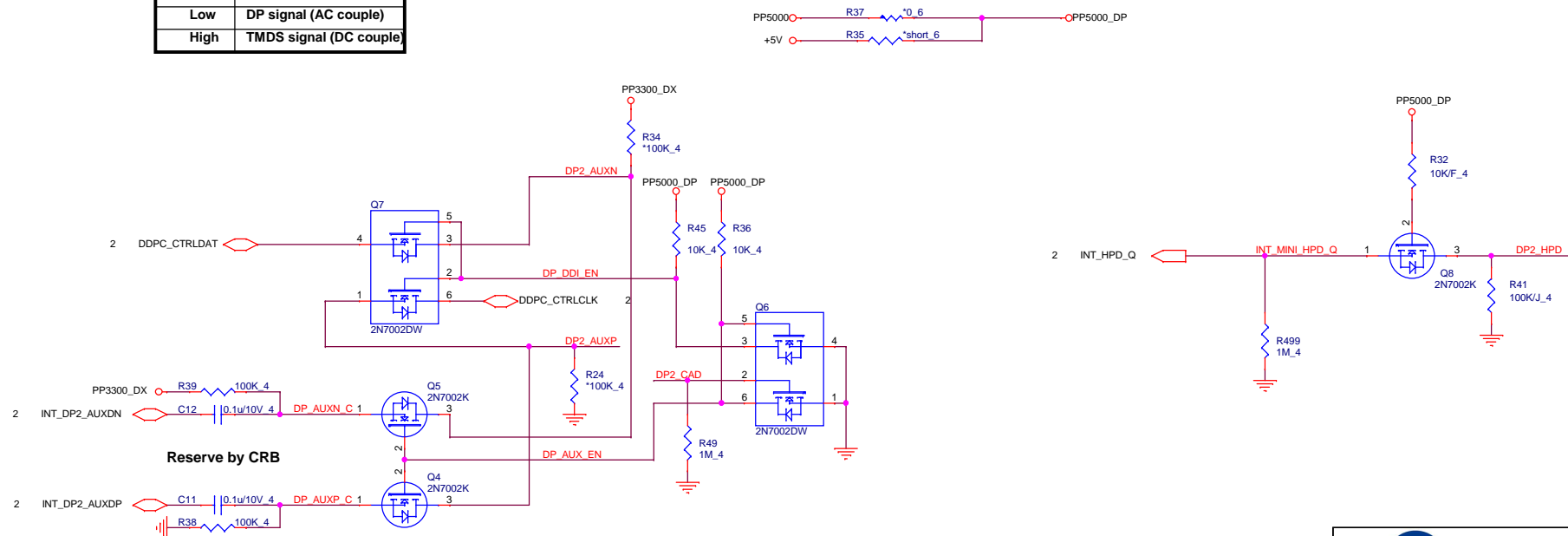


**Layout Notes:**  
Place decoupling CAPs close to Connector



**DP2 AUX (DPP)**

DP_CAD	Behavior
Low	DP signal (AC couple)
High	TMDs signal (DC couple)



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**PROJECT : 0W9**

## DisplayPort

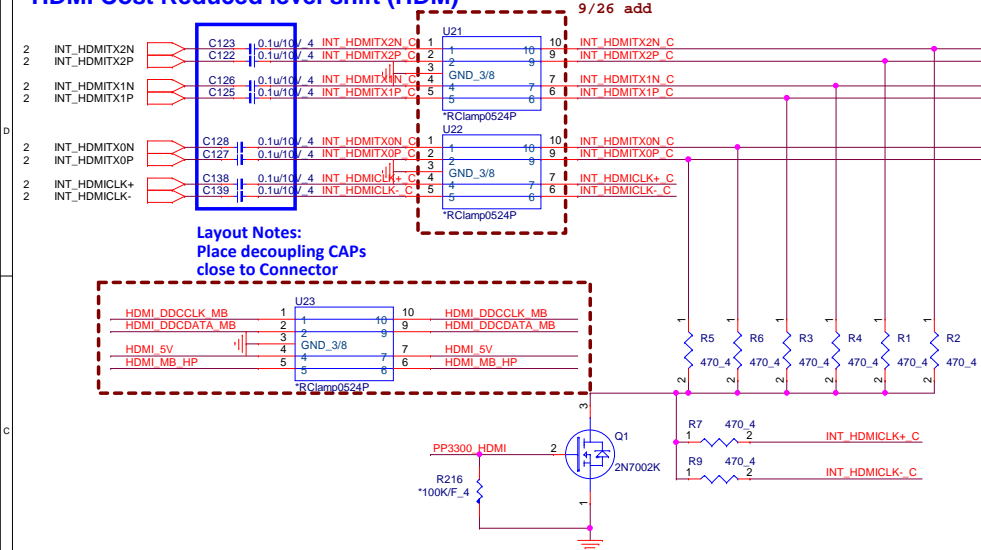
Date: Monday, March 31, 2014

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Rev	A1
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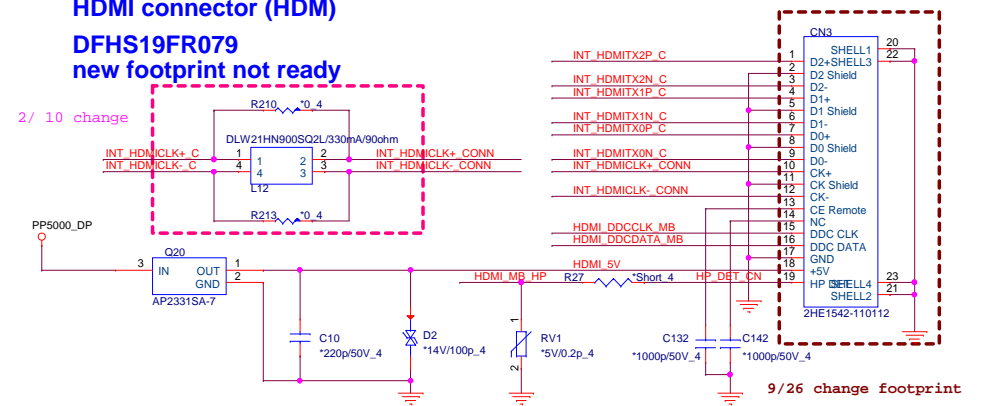


## HDMI Cost Reduced level shift (HDM)

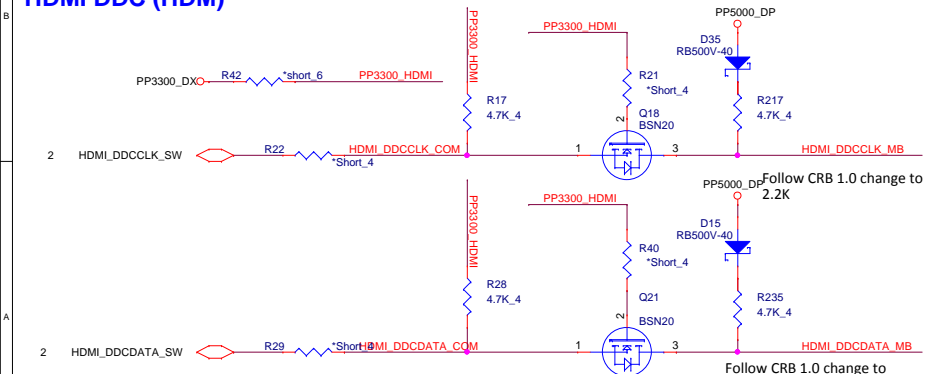


## HDMI connector (HDM)

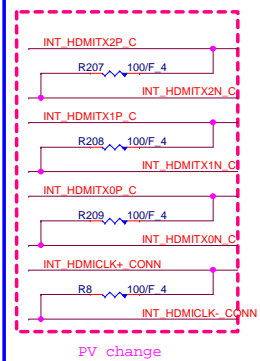
DFHS19FR079  
new footprint not ready



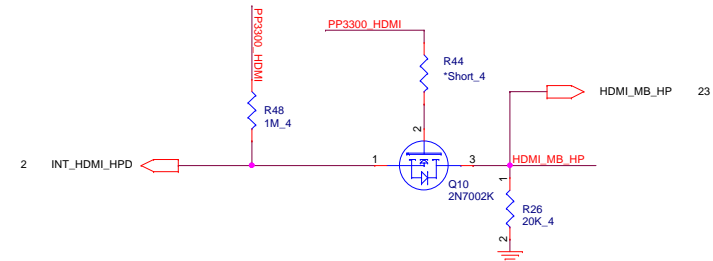
## HDMI DDC (HDM)



## EMI (EMC)



## HDMI-detect (HDM)

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PROJECT : 0W9

## HDMI

Rev  
3A

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	H
Date:	Monday, March 31, 2014

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**+3.3V: 1000mA**  
**+3.3Vaux:330mA**  
**+1.5V:500mA**

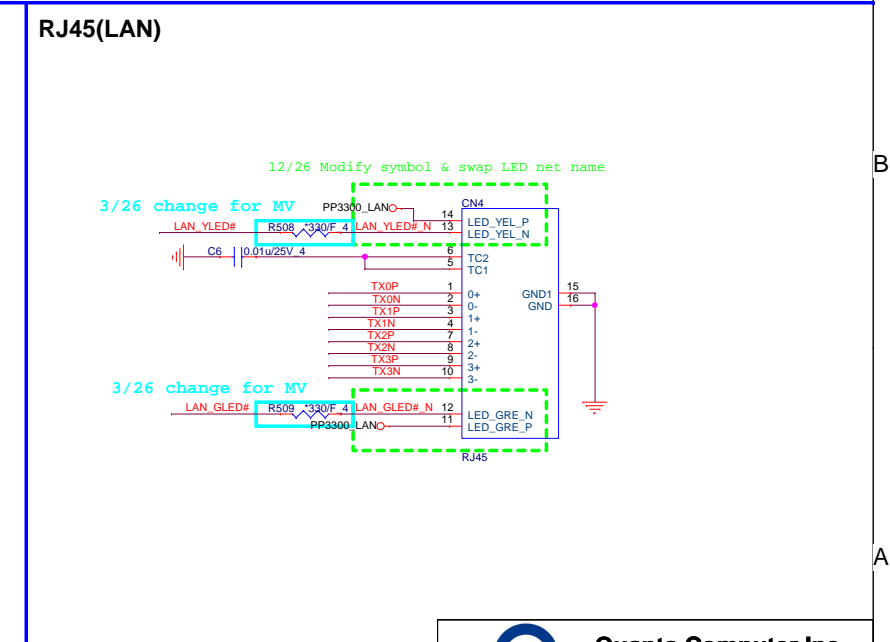
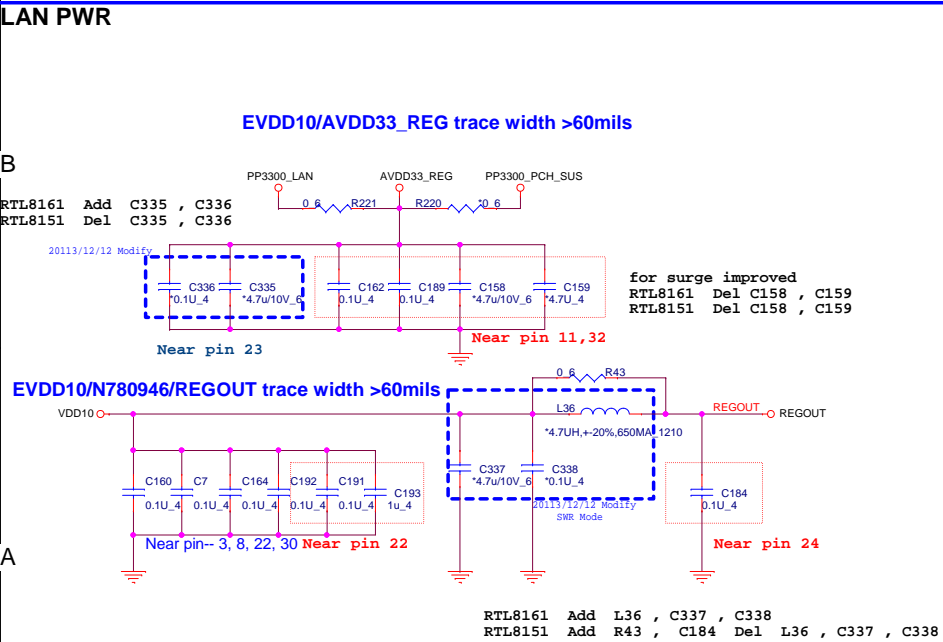
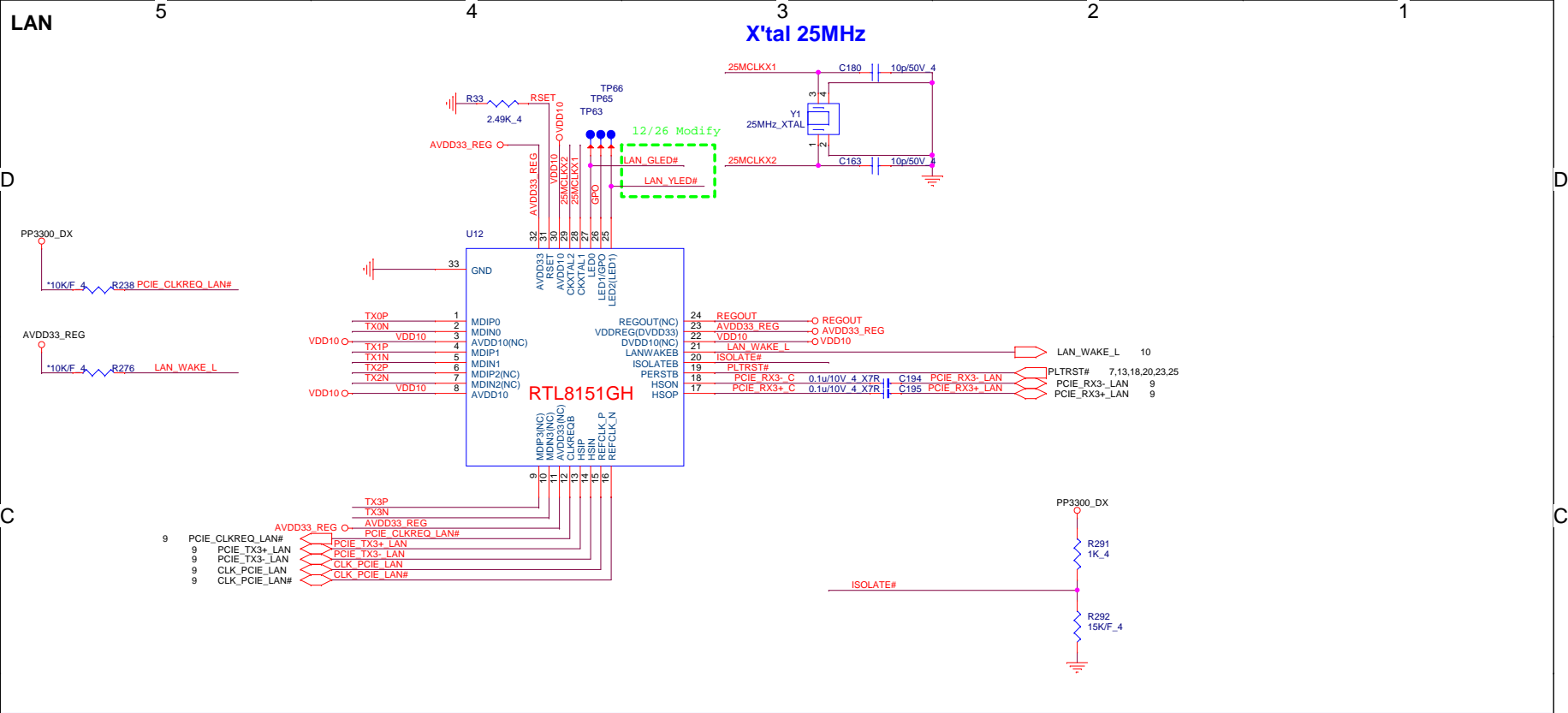


## NGFF SSD connector.

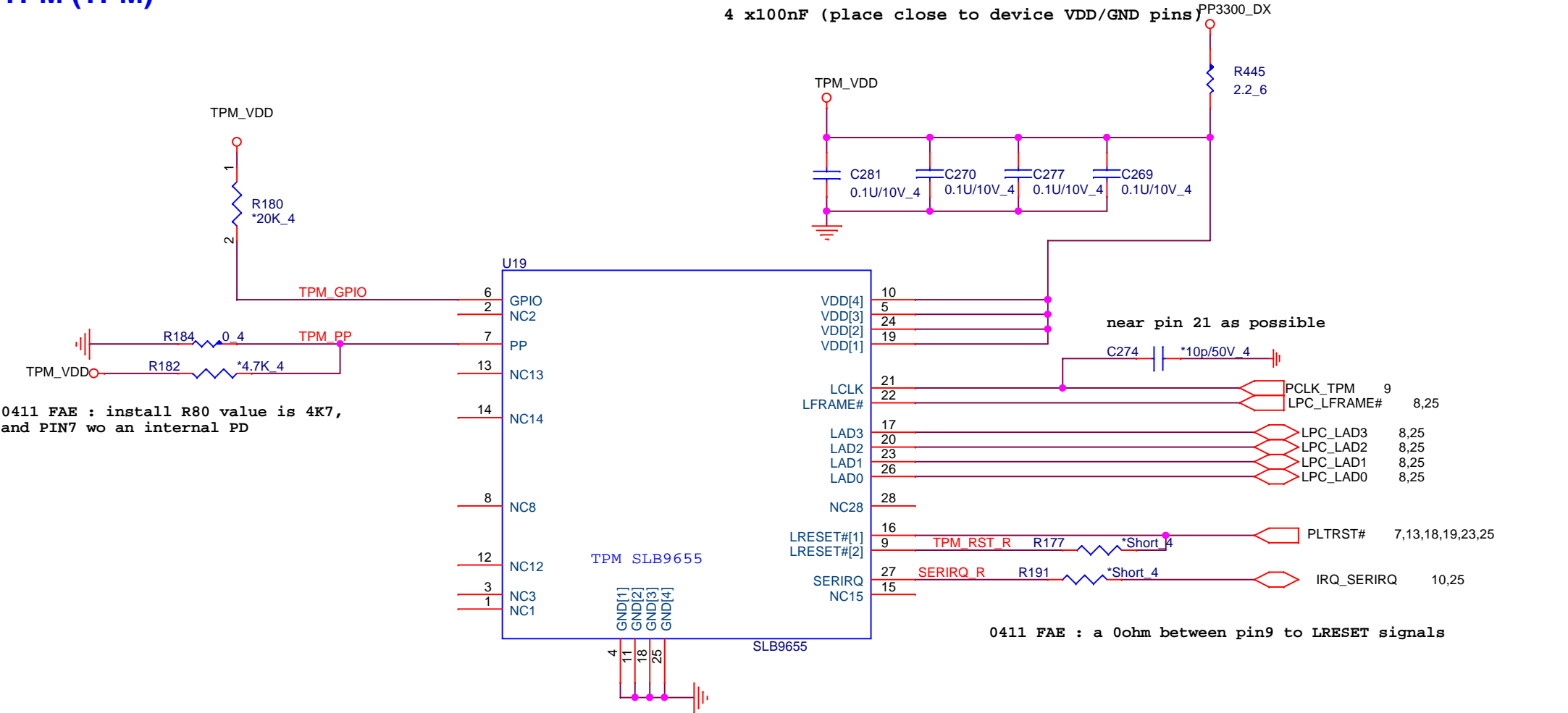



```
rating = 1000mA @ 128G
```

IFDET	Module Type
0	SSD - SATA
1	SSD - PCIE



TPM (TPM)



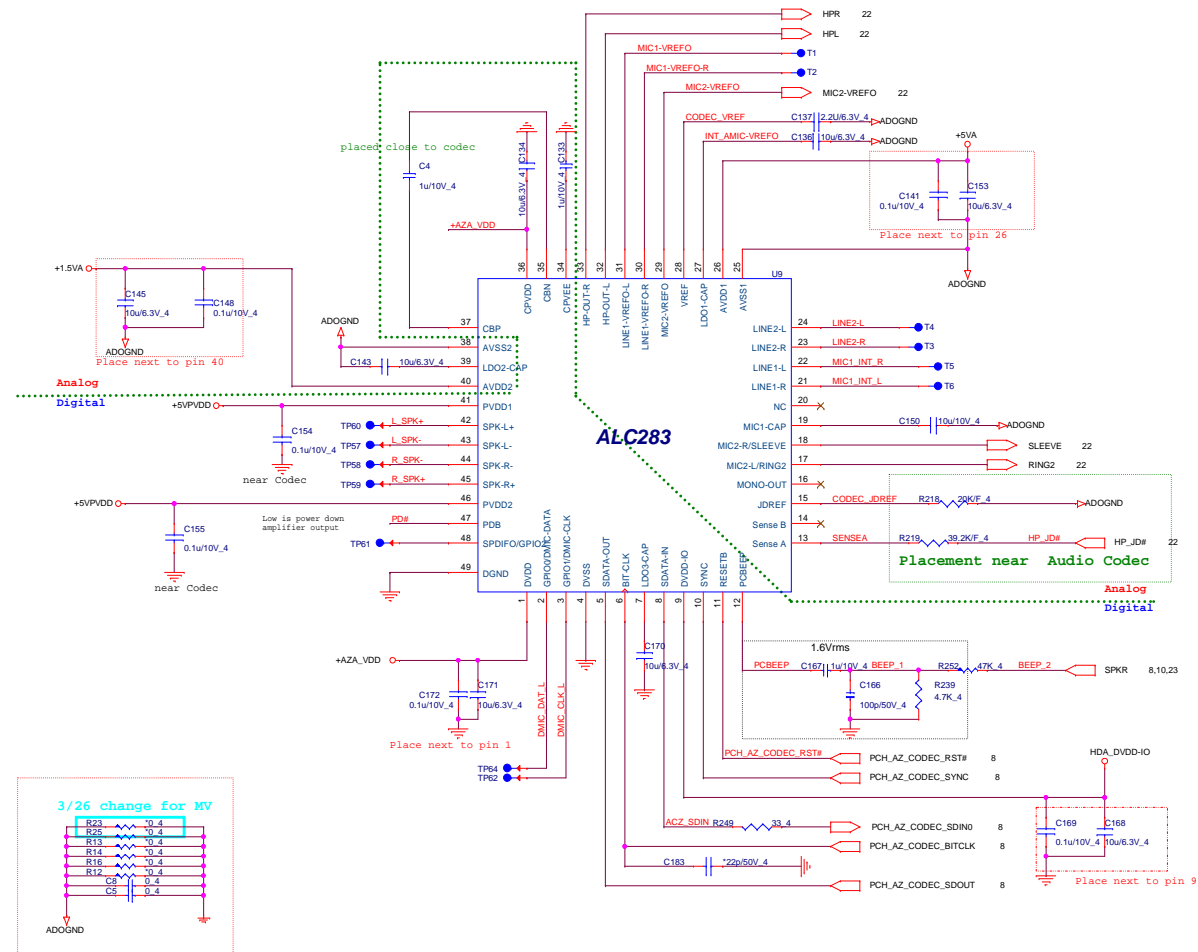


Quanta Computer Inc.

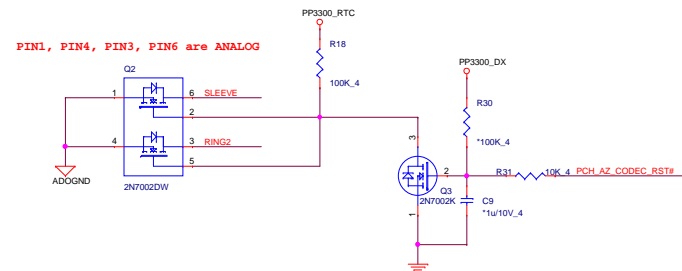
PROJECT : 0W9

Size	Document Number	Rev 3A
TPM SLB9655 / LED		
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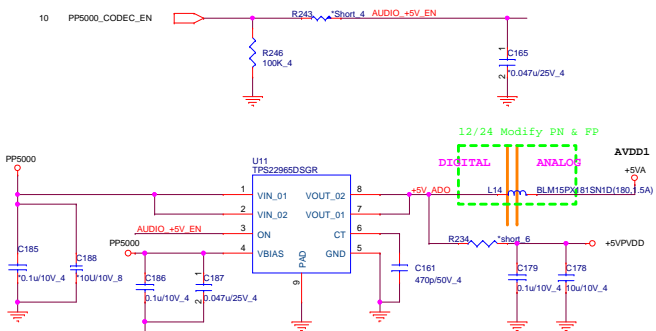
## Codec(ADO)



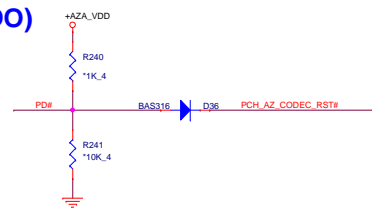
## Grounding circuit(ADO)



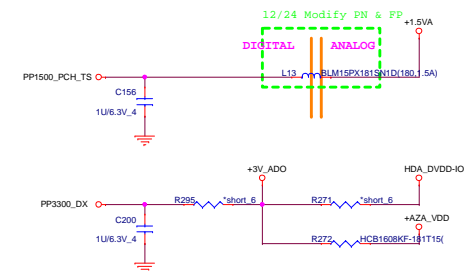
### Codec PWR 5V(ADO)



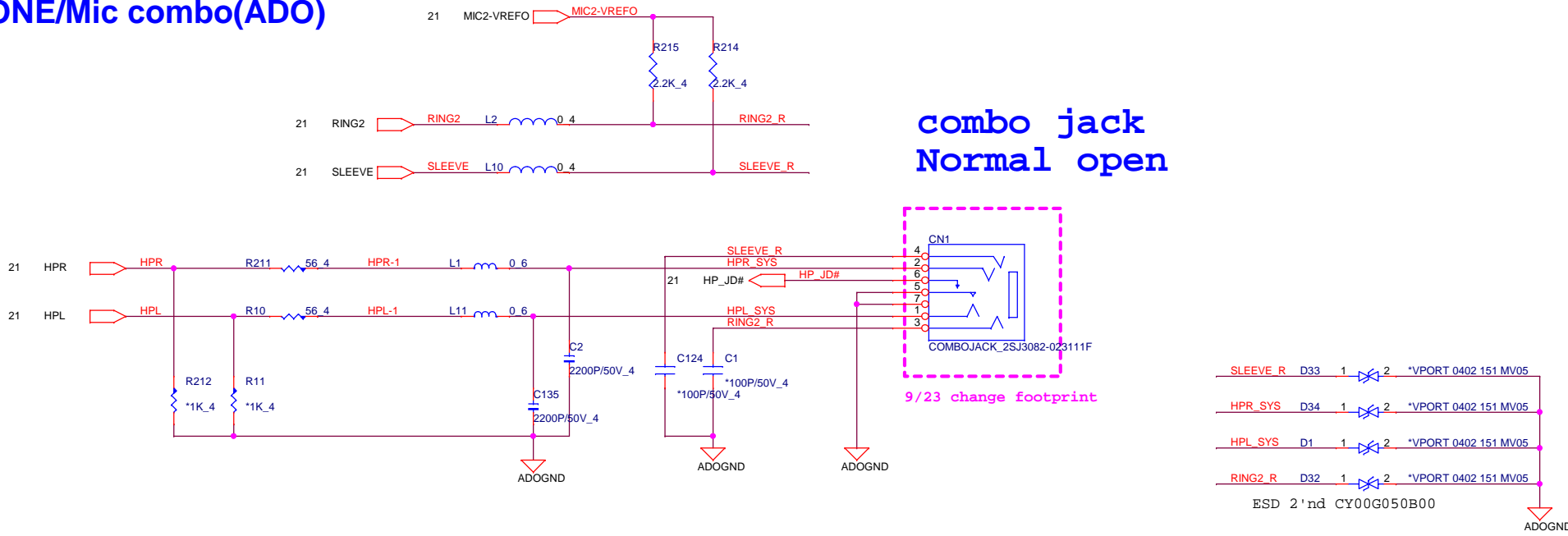
## Mute(ADO)



### Codec PWR 3V/1.5V(ADO)



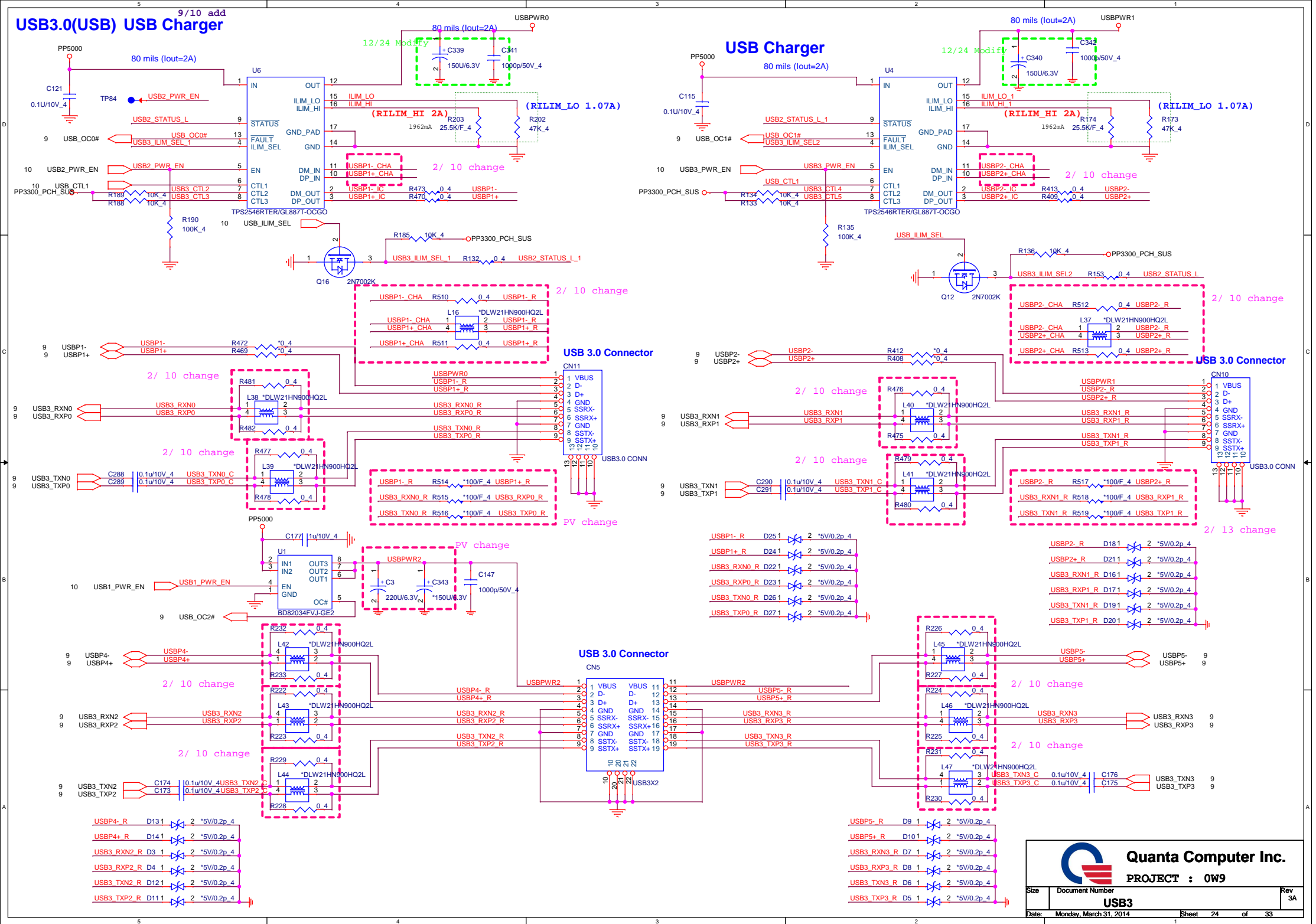
# HEADPHONE/Mic combo(ADO)





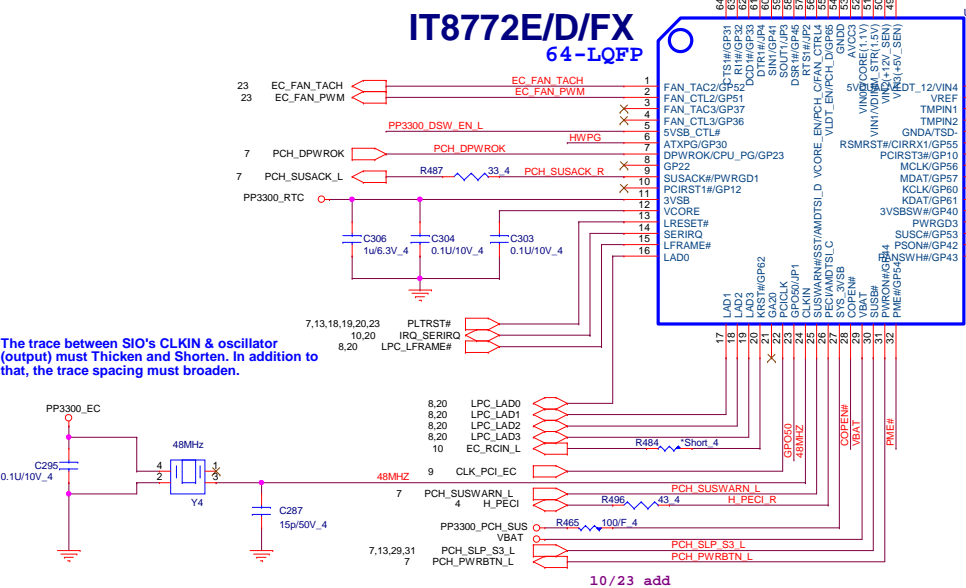
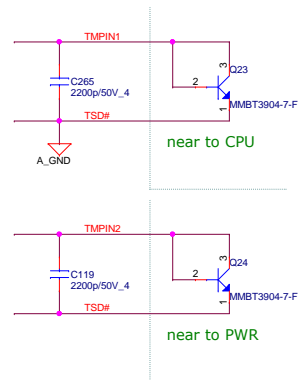
9/10 add

**USB3.0(USB) USB Charger**

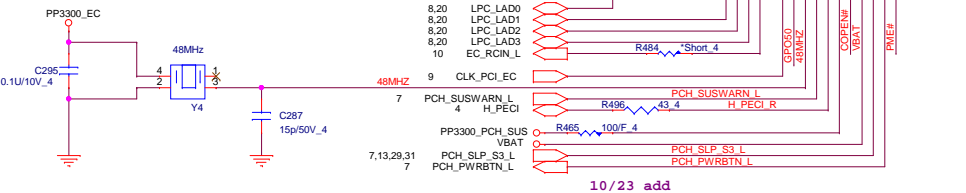




**EC(KBC)**

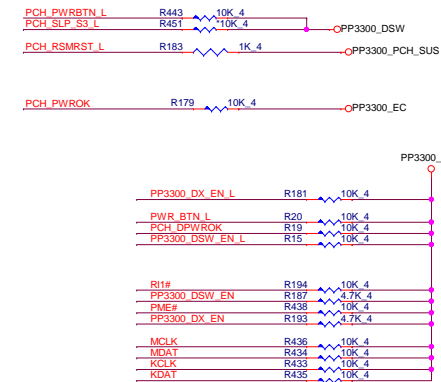
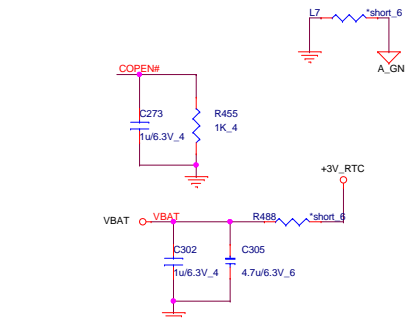
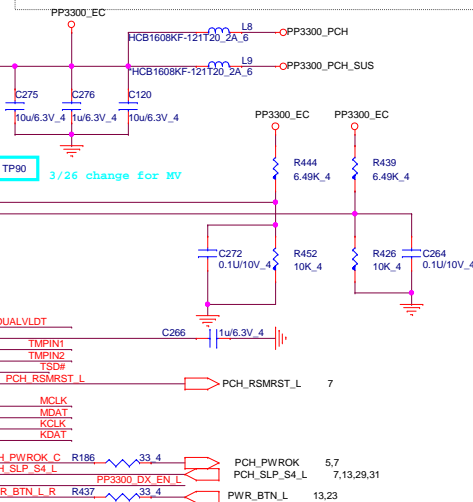


The trace between SIO's CLKIN & oscillator (output) must Thicken and Shorten. In addition to that, the trace spacing must broaden.

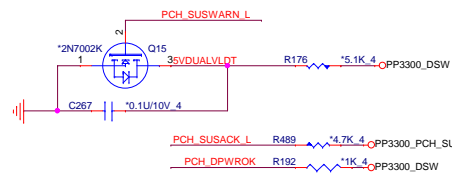
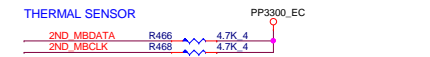


## Power-On Strapping

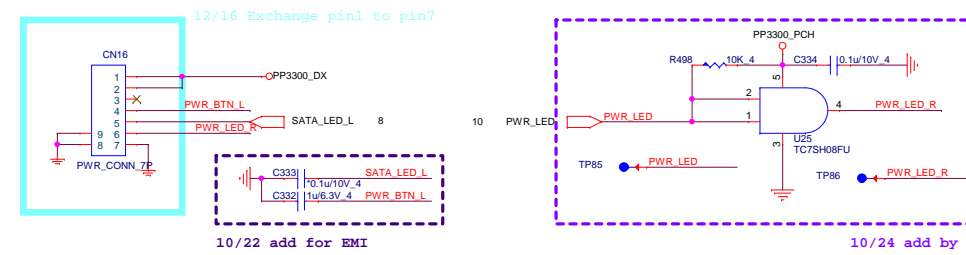
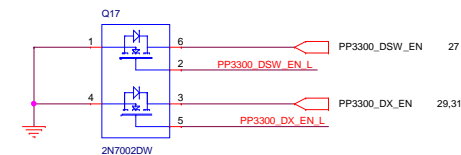
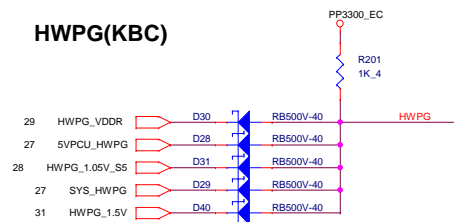
	Symbol	Value	Description
JP1	DSW_EUP_SEL	1	EUP(default)
Pin-23		0	DSW
JP2	WDT_EN	1	Disable_WDT to reset PWROK(default)
Pin-57		0	Enable WDT to reset PWROK
JP3	FAN_CTL_SEL	1	EC Index 68h/73h default = 80h
Pin-59		0	EC Index 68h/73h default = 00h
JP4	K8PWR_EN	1	Disable K8 Power Sequence(default)
Pin-61		0	Enable K8 Power Sequence



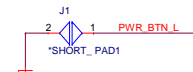
## SM BUS/I2C PU(KBC)



**HWPG(KBC)**



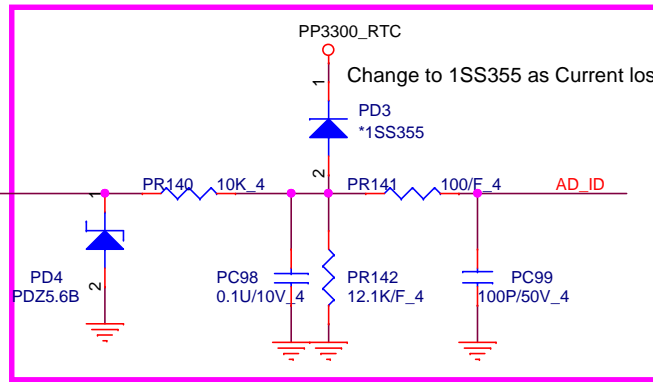
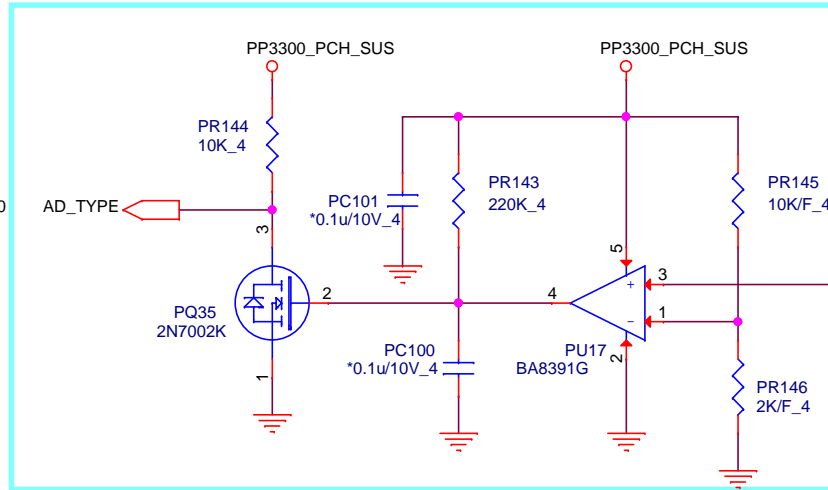
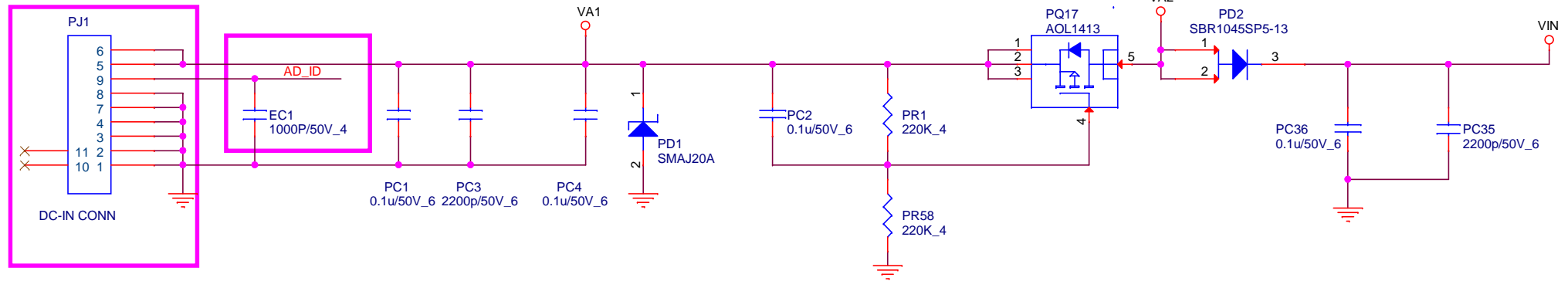
For test only


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	<b>KBC ITE IT8772E</b>	

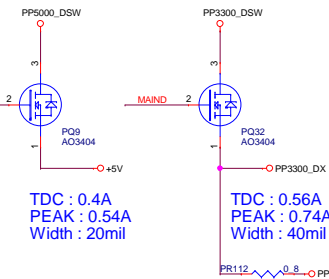
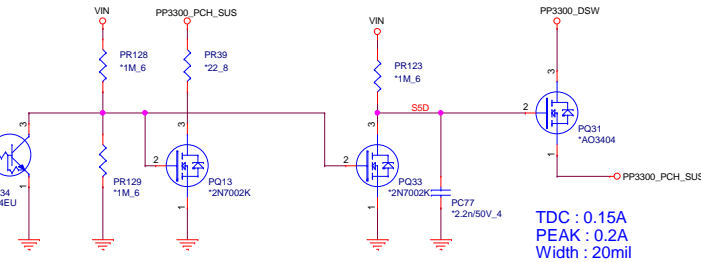
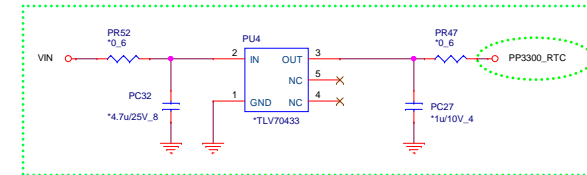
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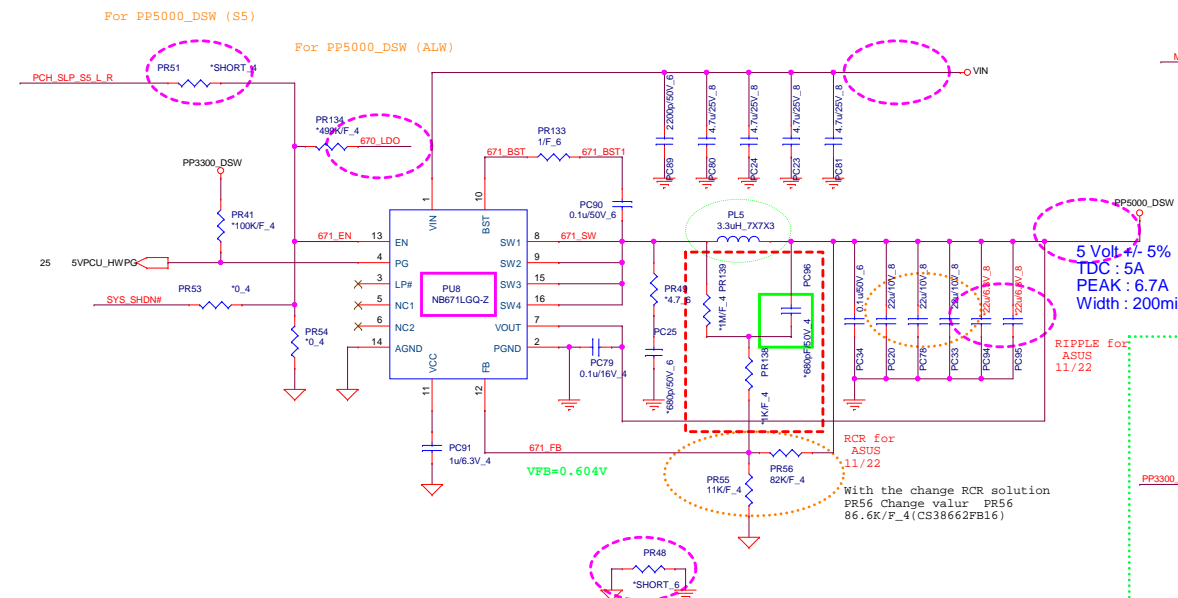
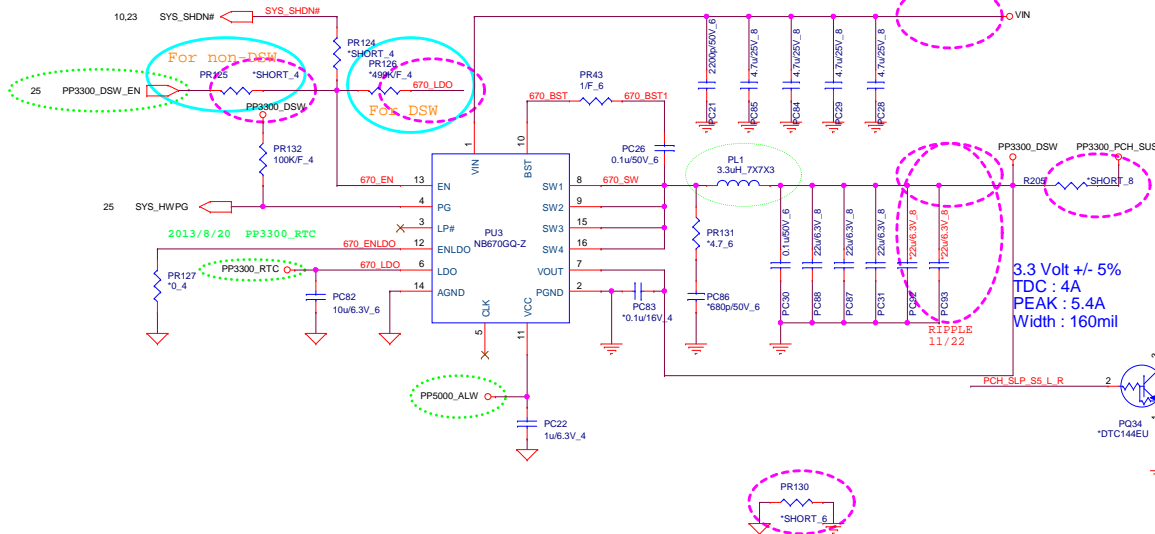
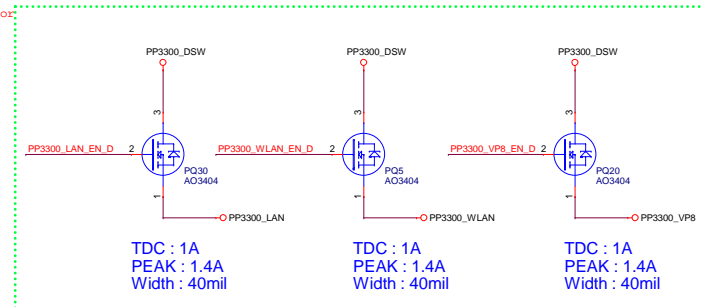
 <b>Quanta Computer Inc.</b> <b>PROJECT : 0W9</b>		Rev
		3A
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	<b>DC-IN</b>	
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PP3300\_LAN\_EN\_D → PP3300\_LAN\_EN\_D 31  
 PP3300\_WLAN\_EN\_D → PP3300\_WLAN\_EN\_D 31  
 PP3300\_VP8\_EN\_D → PP3300\_VP8\_EN\_D 31

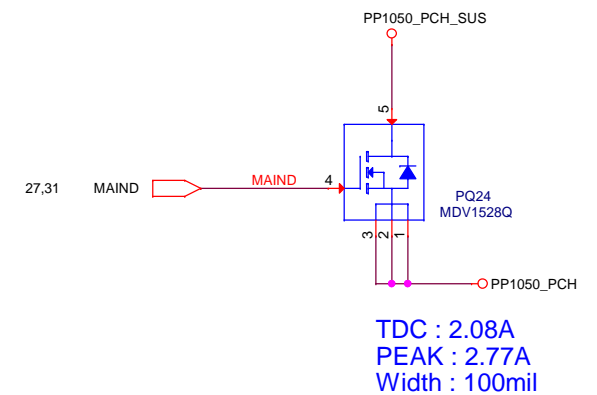
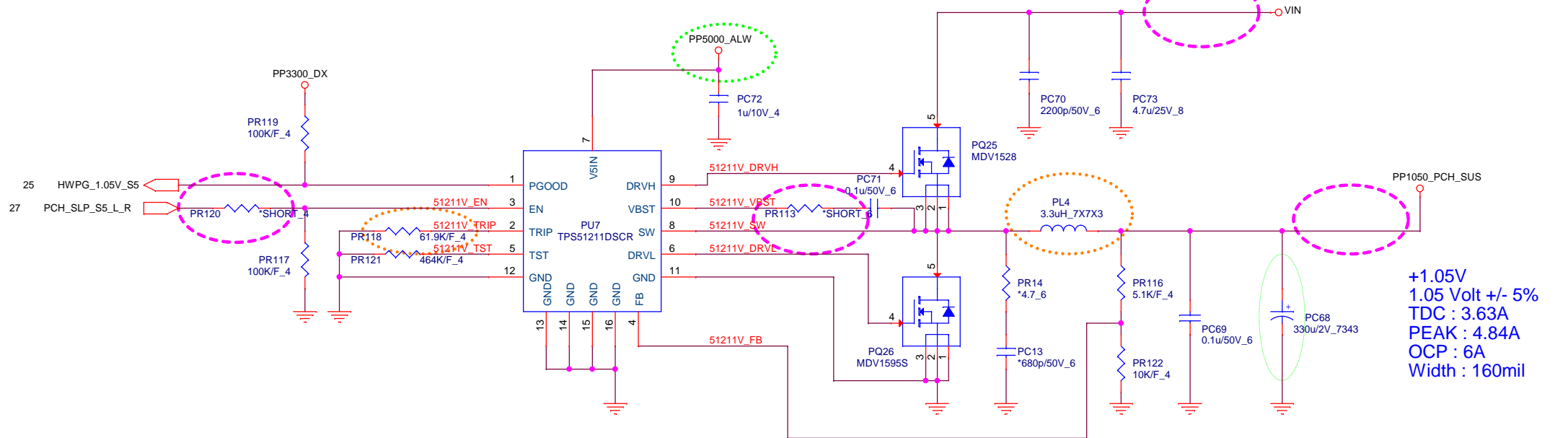
## 2013/8/20 PP3300\_RTC



## 2013/8/20 LAN/WLAN/VP8 decoder



7 PCH\_SLP\_SUS\_L → R491 → PCH\_SLP\_SS\_L → R490 → PCH\_SLP\_SS\_L\_R 28  
 7.13 PCH\_SLP\_SS\_L → PCH\_SLP\_SS\_L → R490 → PCH\_SLP\_SS\_L\_R 28

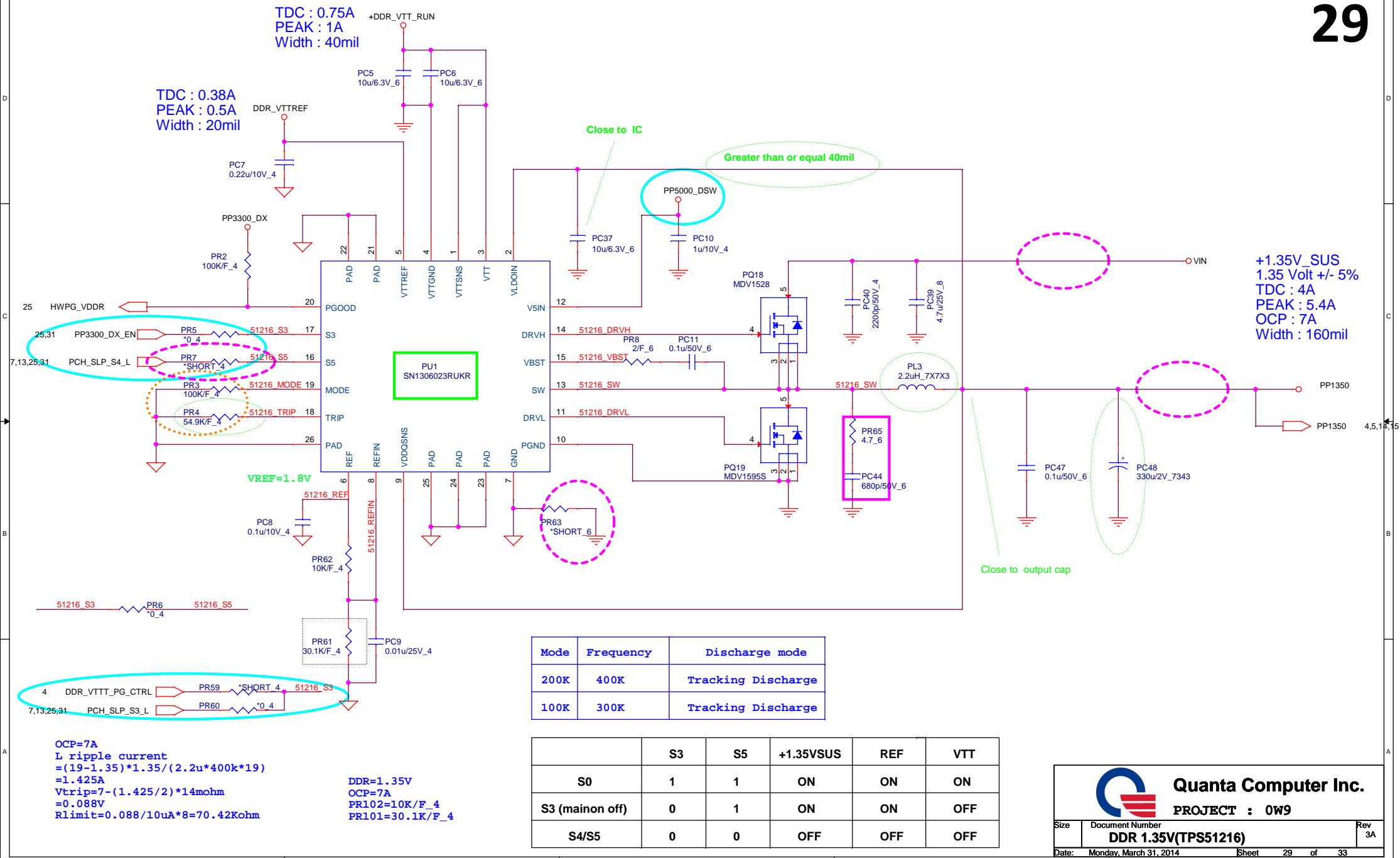


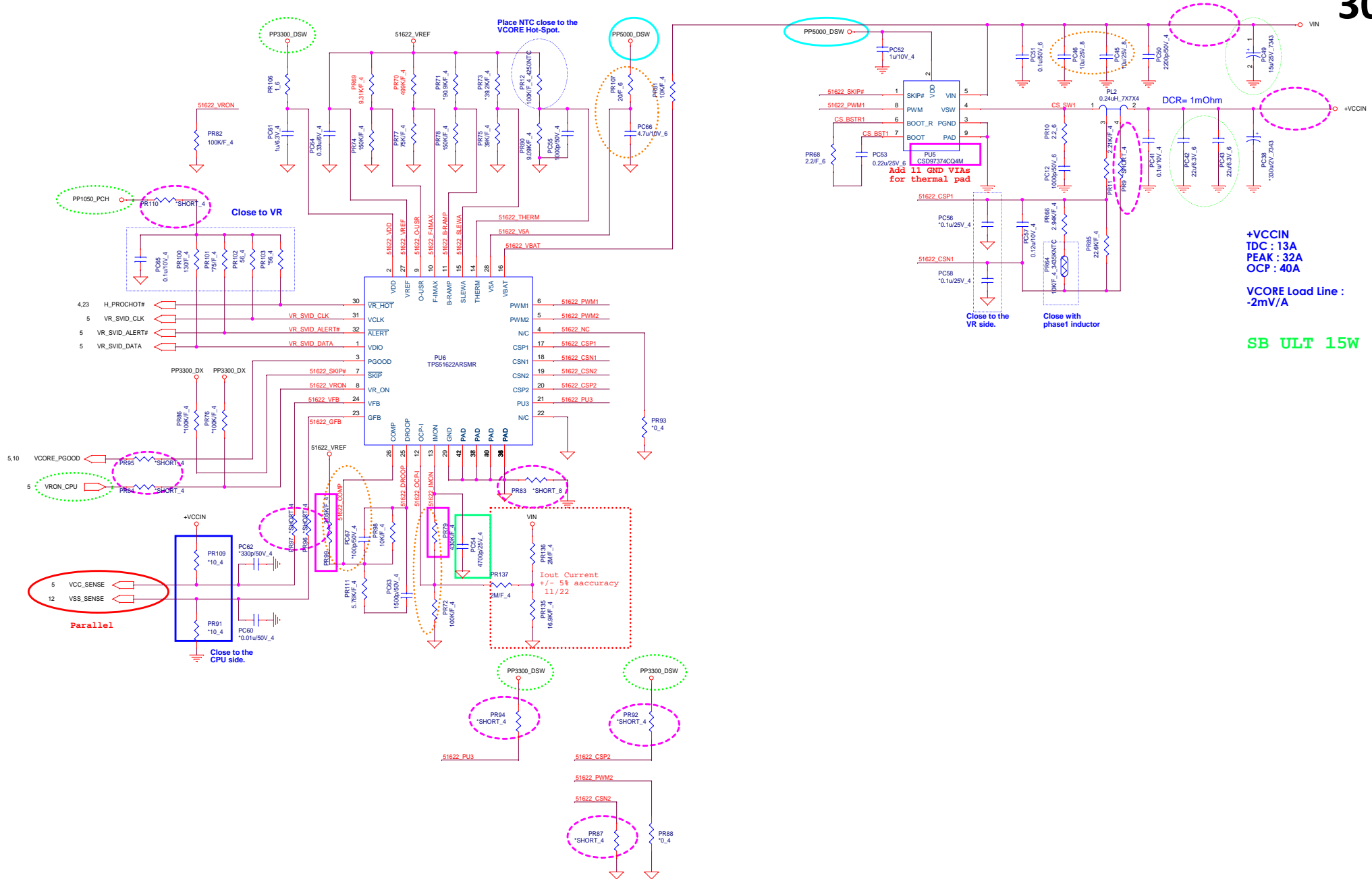
**Quanta Computer Inc.**

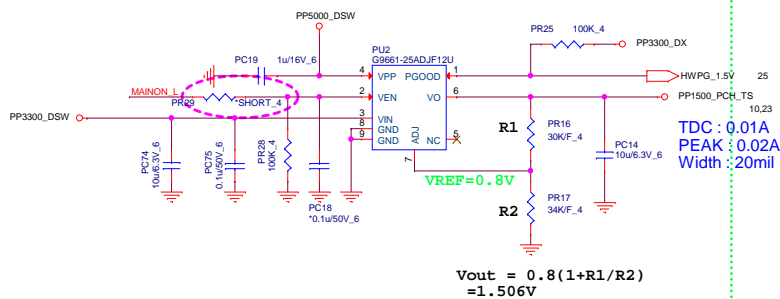
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	<b>+1.05V(TPS51211)</b>	3A

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